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A Novel 15-Level Symmetric Multilevel Inverter With Reduced Switching Devices And THD

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Abstract **- In the recent years, multilevel inverter technology has become popular for medium and high power applications. This paper proposes a 15-level multilevel inverter topology with reduced number of power switches. Simulink model of proposed topology uses 10 MOSFETs,6 diodesand 7 DC sources to produce a stepped output waveform having 15 levels. In comparison toconventional cascaded H-bridge multilevel inverter for 15-level output, 28 switches are needed where as in presented new topology it uses only 10 switches. The presented 15-level multilevel inverter are less costly with reduced switching losses because of reduced number of components, which also leads to a smaller size. In this paper the different Pulse Width Modulation techniques are implemented. The Proposed model is able to achieve low THD in the open loop system and provides superior waveform quality by maintaining ideal sine wave quality. Simulation is done using MATLAB/SIMULINK software.**

Keywords- Multilevel inverter(MLI), Reduced Switching devices, Pulse width modulation(PWM) techniques, Total Harmonic Distortion, MATLAB/SIMULINK

I. INTRODUCTION

Now a days, multilevel inverters has become more popular for medium and high power applications due to its tremendous advantages such as low harmonic distortion, better quality output and for high efficiency compared to two level inverters [1]. Multilevel inverters consist of three important topologies such as neutral clamped multilevel inverter, capacitor clamped multilevel inverter, Cascaded multilevel inverter [2]. The major disadvantage of diode clamped inverter is that as the number of levels increases the required number of clamping diodes increases[3].Voltage unbalancing is the major problem of capacitor clamped inverter and another problem is that as the number of levels increases the required number of flying capacitors also increases[4].Compared to diode clamped and capacitor clamped inverters, cascaded multilevel inverter have gained a major importance due to is advantages such as better output quality, high reliability because of its modular topology. The problem of cascade multilevel inverter is that i. it requires a separate DC source for each H-Bridge, ii. increase in the number of switches as the level increases thus the cost of the system and size of the system increases and it also reduces the efficiency [5]. So a proposed model is developed which uses reduced switching concept thus the cost and size of the system decreases. This Proposed model also reduces THD by controlling the switches using four different pulse width modulation methods such as Equal phases method, half equal phase method, half height method, feed forward method [6]. Simulink model of proposed topology uses 10 MOSFETs,6 diodes and 7 dc sources to produce a stepped output waveform having 15 levels. In comparison to conventional cascaded H-bridge multilevel inverter for 15-level output,28 switches are required where as in presented proposed topology it uses only 10 switches thus the switching losses reduces and the efficiency is improved.

Section II includes the block diagram of proposed topology and in Section III different Pulse width modulation methods for finding switching angles are discussed. Section IV includes switching operation and stepped output of proposed topology. In Section V Simulation results have been made. Lastly, conclusions are made based on Observed results in Section VI.

II. BLOCK DIAGRAM OF PROPOSED TOPOLOGY

Fig. 1. Block diagram of proposed topology

The block diagram of proposed topology is shown in Fig. 1 .It consists of two parts i. level generation part ii. polarity generation part. The level generation part consists of auxiliary switching circuit which are responsible for the generation of levels in positive polarity. The polarity generation part consists of H-bridge circuit which are responsible for the generation of positive polarity of output voltage.

III. PULSE WIDTH MODULATION METHODS FOR FINDING SWITCHING ANGLES

Switching angle is also known as firing angle which is defined as the moment of the voltage level change at the output.

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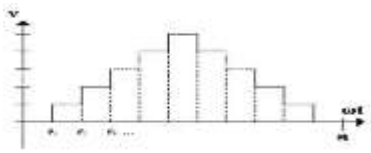

Fig. 2. n-level output waveform

The n-level output waveform is shown in Fig. 2. For n-level output waveform 2(n-1) firing angles are required. We name them as $\theta_1, \theta_2, \theta_3$……. θ_{n-1}. As the sine wave is symmetrical waveform, the negative half cycle (i.e., 180°to 360°) is centrally equal to its positive half cycle (i.e., 0° to 180°). The second quarter period (i.e., 90° to 180°) is mirror symmetrical to the first quarter period (i.e., 0° to 90°) waveform. Firing angles from (i.e., 0° to 90°) is known as main switching angles.
In this proposed topology the different Pulse width modulation methods are implemented [6]to acquire Optimum firing angle. This pulse width modulation method contains four switching patterns along with the corresponding switching by the use of following formulas, they are as follows [7].
Equal phase method(EPM)

$$\theta_k = k * \frac{180}{n} \quad \text{where integer k=1,2,3……..} \frac{n-1}{2} \qquad (1)$$

Half equal phase method(HEPM)

$$\theta_k = k * \frac{180}{n+1} \quad \text{where integer k=1,2,3……..} \frac{n-1}{2} \qquad (2)$$

Half height method(HHM)

$$\theta_k = \sin^{-1}\left(\frac{2k-1}{n-1}\right) \quad \text{where integer k=1,2,3……..} \frac{n-1}{2} \qquad (3)$$

Feed forward method(FFM)

$$\theta_k = \frac{1}{2}\sin^{-1}\left(\frac{2k-1}{n-1}\right) \quad \text{where integer k=1,2,3……..} \frac{n-1}{2} \qquad (4)$$

IV. SWITCHING OPERATION AND STEPPED OUTPUT

The modified 15-level multilevel inverter is shown in Fig. 3 which consists of 7 separate dc sources with reduced number of switches when compared to conventional 15-level cascaded H-bridge multilevel inverter. The proposed model consists of H-bridge formed by 4 MOSFETs and there are 7 dc sources connected to circuit and 6 MOSFETs to regulate the step voltage level across the terminals of the load and the H-bridge is directly connected to a single dc source via diodes. The switches S_i(i=5,6,7,8,9,10) and the diodes (D0,D1,D2,D3, D4,D5) with 6 different DC sources each of equal rating i.e., 40V are connected [8].To produce the initial level of output (Vdc),switches S1 and S4 are fired simultaneously all other switches kept at OFF position. To generate second level output(2Vdc), switches S1, S4 and S10 are fired and all other switches kept OFF position. The switching operation and stepped output of proposed 15-level multilevel inverter is shown in Table 1.

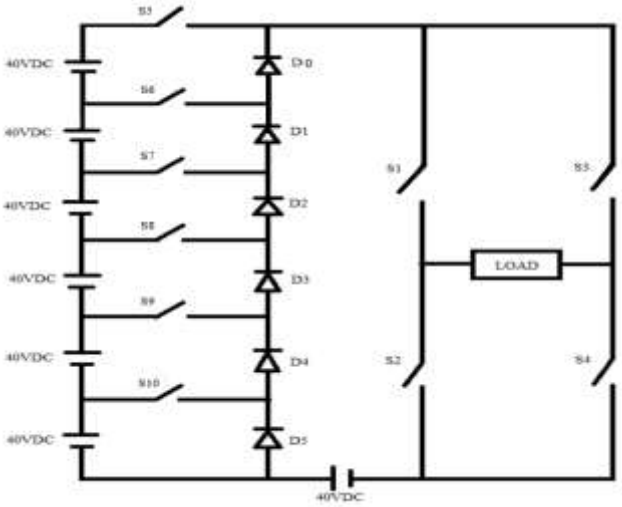

Fig. 3. Proposed multilevel inverter topology

Output	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
Vdc	1	0	0	1	0	0	0	0	0	0
2Vdc	1	0	0	1	0	0	0	0	0	1
3Vdc	1	0	0	1	0	0	0	0	1	1
4Vdc	1	0	0	1	0	0	0	1	1	1
5Vdc	1	0	0	1	0	0	1	1	1	1
6Vdc	1	0	0	1	0	1	1	1	1	1
7Vdc	1	0	0	1	1	1	1	1	1	1
0	1	0	1	0	0	0	0	0	0	0
-Vdc	0	1	1	0	0	0	0	0	0	0
-2Vdc	0	1	1	0	0	0	0	0	0	1
-3Vdc	0	1	1	0	0	0	0	0	1	1
-4Vdc	0	1	1	0	0	0	0	1	1	1
-5Vdc	0	1	1	0	0	0	1	1	1	1
-6Vdc	0	1	1	0	0	1	1	1	1	1
-7Vdc	0	1	1	0	1	1	1	1	1	1

Table 1 Switching operation and stepped output

V. SIMULATION AND RESULTS

The Simulation was done using MATLAB/SIMULINK Software. The Simulink model consists of 10 Power MOSFETs and 6 diodes. In simulation,7 separate dc sources each of equal rating i.e.,40V, various pulse generators are used to fire MOSFET as shown in Fig. 4. By using the Equal phase method**,** the firing angles were calculated and fed to the inverter for its operation. Switches S1,S4,S10,S9,S8,S7,S6 and S5 were fired at delay of 12°,12°,24°,36°,48°,60°,72° and 84° and by using Feed forward method, Switches S1,S4,S10,S9,S8,S7,S6 and S5 were fired at a delay of 2.04°,2.04°,6.18°,10.46°,15°,20°,25.89° and 34.10°and by using Half equal phase method, Switches S1, S4, S10, S9, S8, S7, S6 and S5 were fired at delay of 11.25°,11.25°,22.5°33.75°,45°56.25°,67.5°,78.75°and by using Half height method, switches S1, S4, S10, S9,S8,S7,S6 and S5 were fired at a delay of 4.096°, 4.096°,12.37°,20.9°,30°,40°, 51.78° and 68.2° during first 10 milliseconds of positive half cycle. Similarly firing angle was provided in negative half cycle for next 10 milliseconds except in this case S1 and S4 are replaced by S2 and S3. Output of the model is observed in terms of Voltage and current waveform across load in scope. Pulse

width modulation techniques are used to reduce total harmonic distortion.

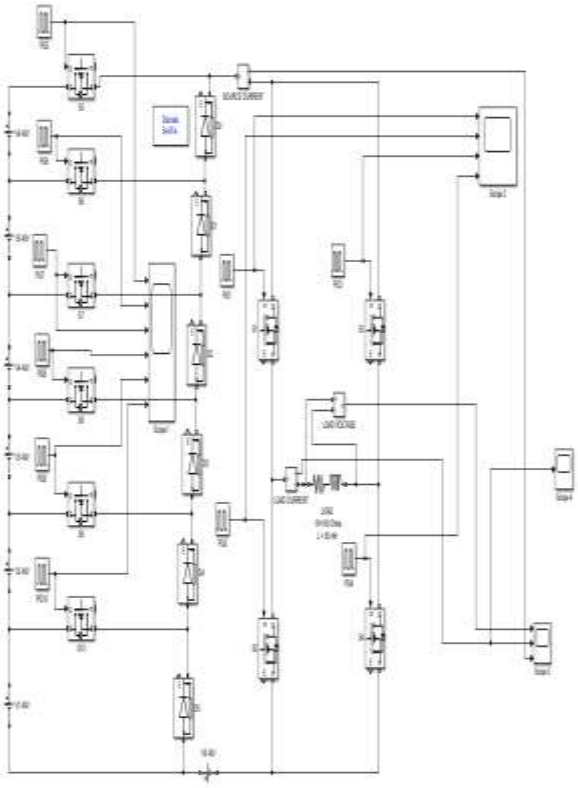

Fig. 4. Simulink diagram of proposed topology

S.NO	VOLTAGE OUTPUT		Load VOLTAGE
	SWITCHES ON	SWITCHES OFF	
1	S2 S3 S10 S9 S8 S7 S6 S5	S1 S4	200
2	S2 S3 S10 S9 S8 S7 S6	S1 S4 S5	100
3	S2 S3 S10 S9 S8 S7	S1 S4 S5 S6	200
4	S2 S3 S10 S9 S8	S1 S4 S5 S6 S7	100
5	S2 S3 S10 S9	S1 S4 S5 S6 S7 S8	129
6	S2 S3 S10	S1 S4 S5 S6 S7 S8 S9	99
7	S2 S3	S1 S4 S5 S6 S7 S8 S9 S10	49
8	S2 S3	S2 S4 S5 S6 S7 S8 S9 S10	0
9	S2 S4	S2 S3 S5 S6 S7 S8 S9 S10	49
10	S2 S4 S10	S2 S3 S5 S6 S7 S8 S9	99
11	S2 S4 S10 S9	S2 S3 S5 S6 S7 S8	129
12	S2 S4 S10 S9 S8	S2 S3 S5 S6 S7	100
13	S2 S4 S10 S9 S8 S7	S2 S3 S5 S6	200
14	S2 S4 S10 S9 S8 S7 S6	S2 S3 S5	100
15	S2 S4 S10 S9 S8 S7 S6 S5	S2 S3	200

Table 2 Proposed MLI Switching states and Outputs

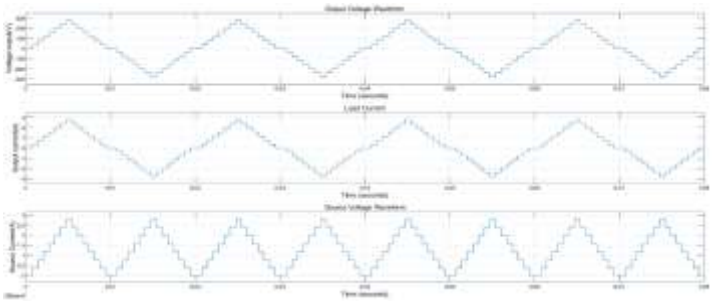

Fig. 5. Output waveform with R-load using Equal Phase Method(EPM)

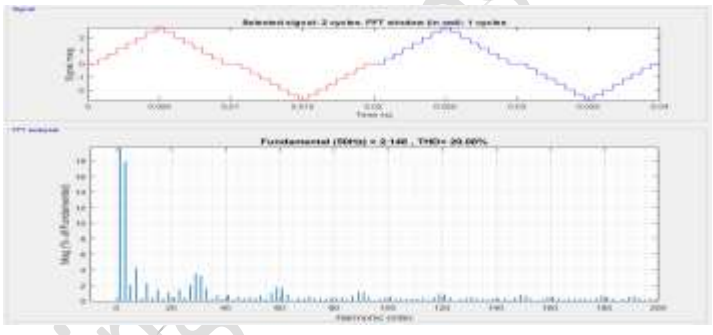

Fig. 6. THD of current waveform on R-load of 100ohms using EPM

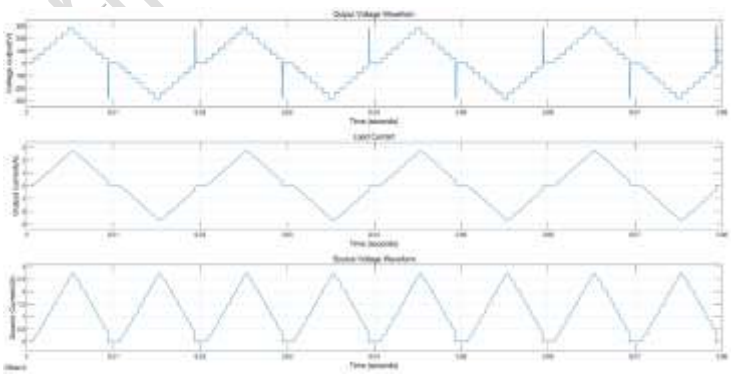

Fig. 7. Output waveform with RL-load using Equal Phase Method(EPM)

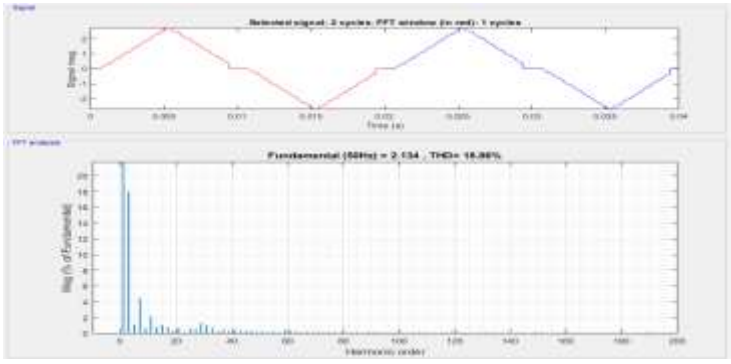

Fig. 8. THD of current waveform on RL-load using EPM

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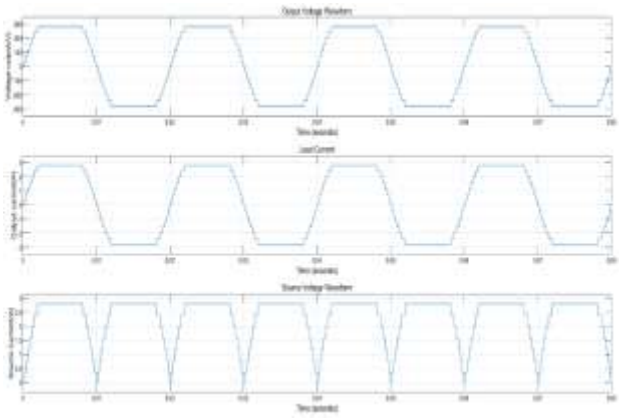

Fig. 9. Output waveform with R-load using Feed Forward Method(FFM)

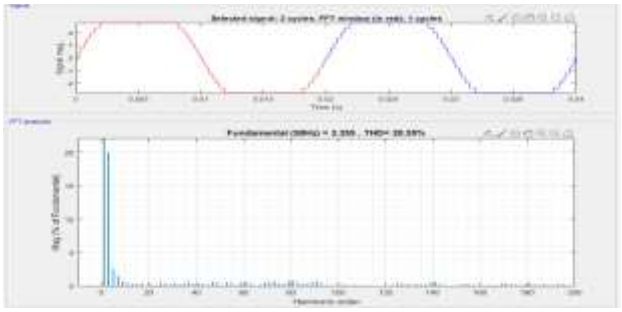

Fig. 10. THD of current waveform on R-load of 100ohms using FFM

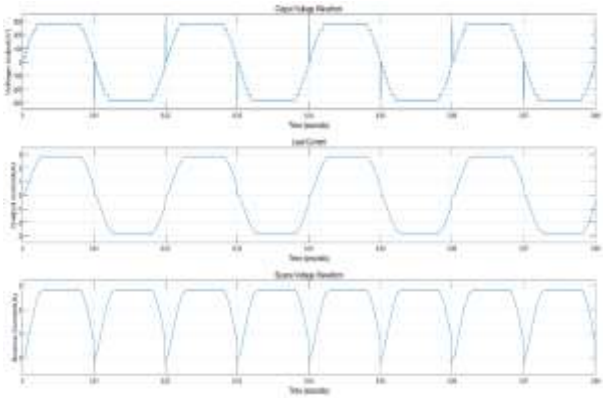

Fig. 11. Output waveform with RL-load using Feed Forward Method(FFM)

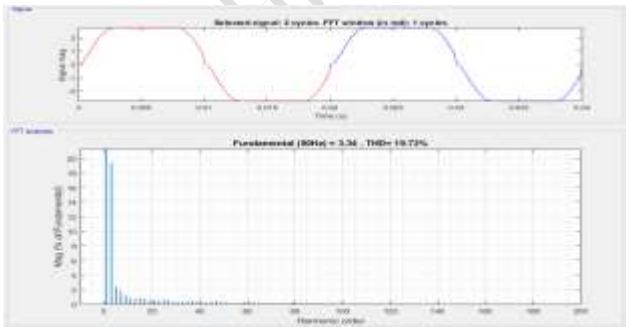

Fig. 12. THD of current waveform on RL-load using FFM

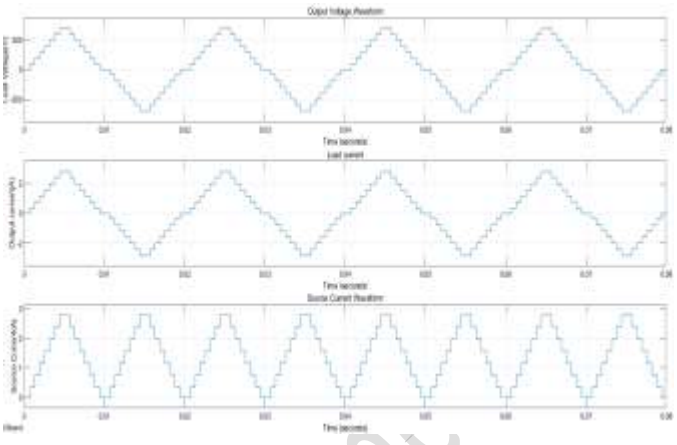

Fig. 13. Output waveform for R-load using Half Equal Phase Method(HEPM)

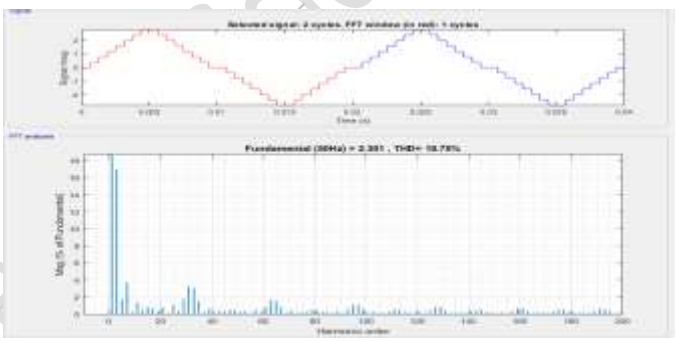

Fig. 14. THD of current waveform on R-load of 100ohms using HEPM

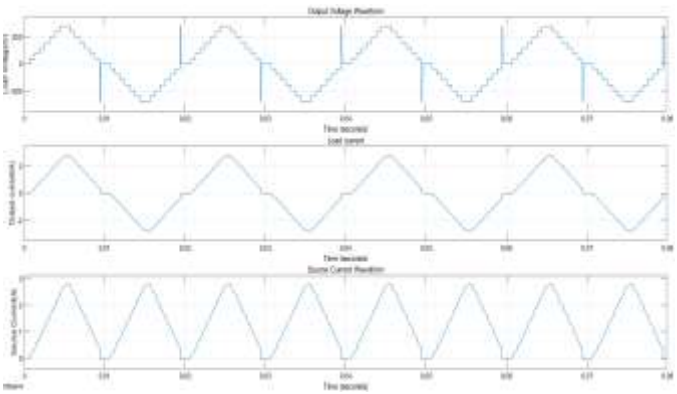

Fig. 15. Output waveform for RL-load using Half equal phase method(HEPM)

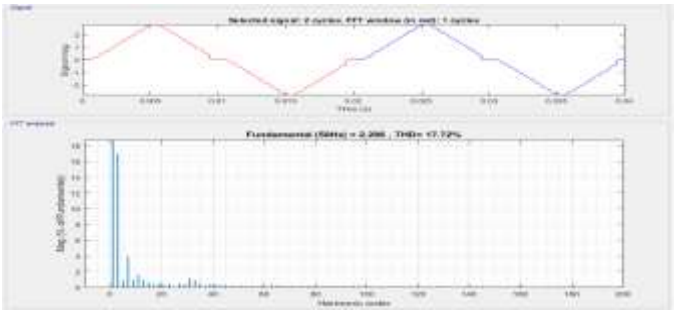

Fig. 16. THD of current waveform on RL-load using HEPM

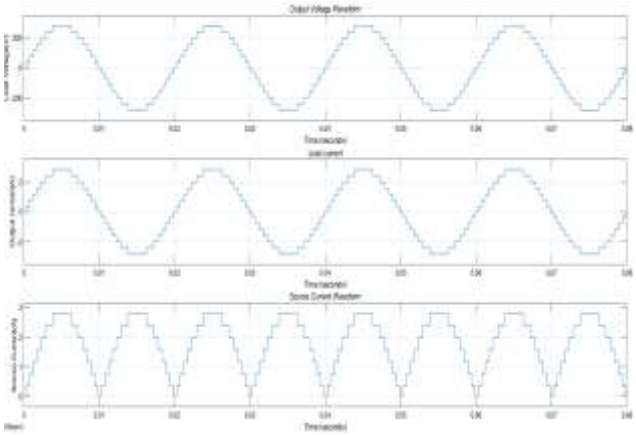

Fig. 17. Output waveform for R-load using Half Height Method(HHM)

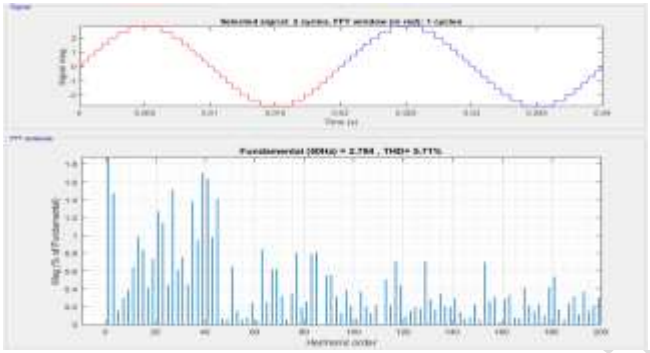

Fig. 18. THD of current waveform on R-load of 100ohms using HHM

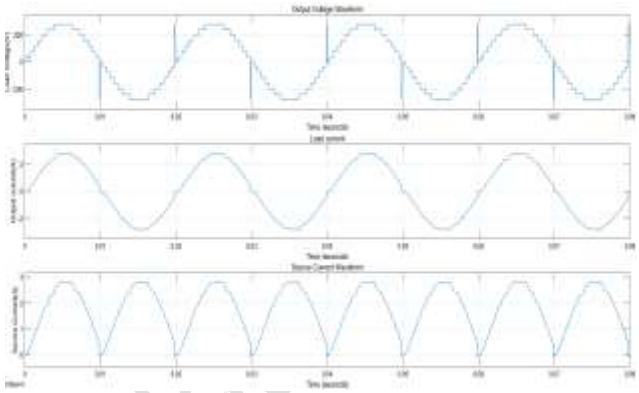

Fig. 19. Output waveform for RL-load using Half Height Method(HHM)
THD Analysis

Methods to calculate Switching angle for 15-level MLI	%THD for R-load	%THD for RL-load
Feed Forward Method	20.55%	19.73%
Equal Phase Method	20.08%	18.86%
Half Equal Phase Method	18.75%	17.72%
Half Height Method	5.71%	3.51%

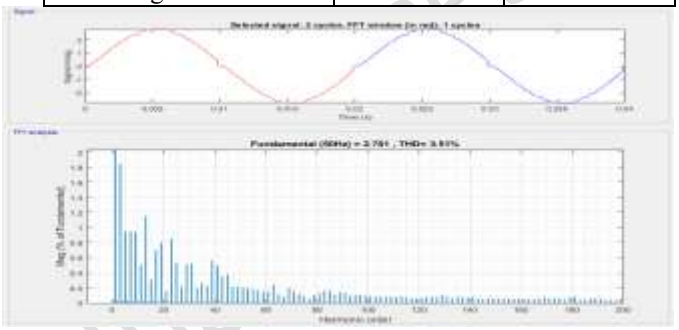

Fig. 20 THD of current waveform on RL-load using HHM

IV. CONCLUSION

Multilevel inverters by using reduced switching concept, and we observed their level output waveforms. Total Harmonic Analysis of the output current waveform value of the inverter is measured using FFT analysis by MATLAB Powergui box. Simulation results were observed in output response in terms of voltage and current waveforms across the R-load and RL load. R-load was of 100 ohms, RL load was of 100 Ohms and 30 mH .In RL Load sinusoidal nature of current due to the presence of inductance in the circuit. In this paper Equal phase method, Half equal phase method, Half Height method and Feed Forward methods have been proposed to find switching angles for modified 15-level cascade H-bridge multilevel inverter. From Table 3 it can be concluded that by Half Height method we obtained better harmonic spectrum i.e., 5.71% for R-load and 3.51% for RL-load when compared to other three methods, and the output waveform obtained by Half Height method is nearer to the sinusoidal. The results were obtained by using Matlab/Simulink to validate the design.

Table 3 Comparison of THD using different PWM techniques

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