1

12-09-2016,

Hyderabad

To
The Principal,
GNITS,
Hyderabad.

Sub: Request for advance amount of Rs. 25,000/- for conduct one week workshop on "Functional Approach to VLSI Design" during 17-09-2016 to 22-10-2016. Regd...

Respected sir,

I, Dr.K.Ragini, Professor and Mrs.Deepthi Amuru, Assistant Professor of ECE Department have planned for a one week workshop on "Functional Approach to VLSI Design " from 17/10/2016 to 22/10/2016 for the teaching faculty of Engineering colleges in Technical collaboration with IETE Chapter, Hyderabad. We request to sanction an amount of Rs. 25,000/- as an advance from the budget amount of Rs.54,000/-. Kindly consider and do the needful.

Thanking you sir,

Yours faithfully,

K. Ragini

Dr.K.Ragini,
Course Coordinator

Mrs. Deepthi Amuru
Co-Course Coordinator

Grams: GI

2

PH : Office : 3565649
PBX : 3566803,3565648
Fax : 040-3564187
Email : principal@gnits.ac.in
admin@gnits.ac.in
Website : www.gnits.ac.in

G.NARAYANAMMA INSTITUTE OF TECHNOLOGY & SCIENCE
(FOR WOMEN)
(SPONSORED BY G. PULLA REDDY CHARITABLE TRUST, HYDERBAD)
(APPROVED BY AICTE AND AFFILIATED TO JNTUNIVERSITY)
SHAIKPET, HYDERABAD - 500008. (AP)

Dt: 04-10-16
Hyderabad.

To
Dr.M.Satyam
Retd. Professor, IISC Bangalore
& Professor, Vasavi College of Engineering
Hyderabad.

Respected Sir,

Sub: Request to be the chief guest for the workshop on "**Functional Approach to VLSI Design**" organized by ECE dept, GNITS in collaboration with IETE, Hyderabad chapter-regarding.

The Electronics & Communication Engineering Department of G. Narayanamma Institute of Technology & Science is organizing an one week workshop on "Functional Approach to VLSI Design" during 17th to 22nd Oct -2016.

We earnestly request you to be the **Chief Guest** and deliver the **Key note address** from 9.45 to 11.00 AM on 17th October, 2016.

We would be grateful to you for sparing your valuable time to make our program a grand success.

Thanking you.

Dr. B. Venkateshulu
HOD, ECE

☎ : 040-23565648 / 49
Fax: 040-23564187

rtified Institution

G. NARAYANAMMA INSTITUTE OF TECHNOLOGY & SCIENCE

Accredited by NAAC of UGC upto 20-02-2019 (For Women)
(Sponsored by G. Pulla Reddy Charities Trust, Hyderabad.)
(Accredited by NBA (from May 2007 to April 2010) Approved by AICTE & Affiliated to J N T U H)
8-1-297/2/I, Shaikpet, Hyderabad - 500 104. T.S. INDIA
E-mail : principal@gnits.ac.in, Website : www.gnits.ac.in

Dt: 03-11-16
Hyderabad.

To
Dr.G.Laxmi Narayana
IETE Chairman, Hyderabad chapter
& Principal, Anurag College of Engineering
Hyderabad.

Respected Sir,

G.Narayanamma Institute of Technology and Science(for women) whole heartedly appreciates your acceptance as **Guest of honor** and delivering a lecture - **"Frequency consideration for chip design"** on 17/10/2016 for the one week workshop on **"Functional Approach to VLSI Design"** conducted in the Department of ECE from 17/10/2016 to 22/10/2016.

We are very happy to inform you that your lecture has been one of the very best. We thank you for your wonderful lecture and supporting us in knowledge sharing.

Wishing you all the best for future endeavors.

With regards,

Dr.K.Ramesh Reddy,
Principal,
GNITS

Principal
G. Narayanamma Institute of
Technology & Science (for women)
Shaikpet, Hyderabad - 500 104.

Estd : 1997
Grams : GNITS
AN ISO 9001 : 2008 Certified Institution

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E-mail : principal@gnits.ac.in, Website : www.gnits.ac.in

Dt: 03-11-16
Hyderabad.

To
Dr.P.A.Govindacharyulu,
Professor, Dept. of ECE,
Vasavi College of Engineering,
Hyderabad.

Respected Sir,

G.Narayanamma Institute of Technology and Science(for women) whole heartedly appreciates your acceptance as **Resource person** and delivering a lecture - **"Analog Mixed signal design flow"** on 19/10/2016 for the one week workshop on **"Functional Approach to VLSI Design"** conducted in the Department of ECE from 17/10/2016 to 22/10/2016.

We are very happy to inform you that your lecture has been one of the very best. We thank you for your wonderful lecture and supporting us in knowledge sharing.

Wishing you all the best for future endeavors.

With regards,

Dr.K.Ramesh Reddy 3/11/16
Principal,
GNITS

Principal
G. Narayanamma Institute of
Technology & Science (for woman)
Shaikpet, Hyderabad - 500 104.

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E-mail : principal@gnits.ac.in, Website : www.gnits.ac.in

Dt: 03-11-16
Hyderabad.

To
Dr.N.Siva Shankar Reddy,
Assoc.Professor, Dept. of ECE,
Vasavi College of Engineering,
Hyderabad.

Respected Sir,

G.Narayanamma Institute of Technology and Science(for women) whole heartedly appreciates your acceptance as **Resource person** and delivering a lecture - **"Techniques for Low Power Design"** on 18/10/2016 for the one week workshop on **"Functional Approach to VLSI Design"** conducted in the Department of ECE from 17/10/2016 to 22/10/2016.

We are very happy to inform you that your lecture has been one of the very best and got an excellent feedback. We thank you for your wonderful lecture and supporting us in knowledge sharing.

Wishing you all the best for future endeavors.

With regards,

3/11/16

Dr.K.Ramesh Reddy,
Principal,
GNITS

Principal
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Shaikpet, Hyderabad - 500 104.

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E-mail : principal@gnits.ac.in, Website : www.gnits.ac.in

Dt: 03-11-16
Hyderabad.

To
Dr.N.S.Murthy,
Professor, Dept. of ECE,
Vasavi College of Engineering,
Hyderabad.

Respected Sir,

G.Narayanamma Institute of Technology and Science(for women) whole heartedly appreciates your acceptance as **Resource person** and delivering a lecture - **"System level power optimization"** on 21/10/2016 for the one week workshop on "**Functional Approach to VLSI Design**" conducted in the Department of ECE from 17/10/2016 to 22/10/2016.

We are very happy to inform you that your lecture has been one of the very best. We thank you for your wonderful lecture and supporting us in knowledge sharing.

Wishing you all the best for future endeavors.

With regards,

7/11/16

Dr.K.Ramesh Reddy,
Principal,
GNITS

G. Narayanamma Institute of Technology & Science (For Women), Shaikpet, Hyd - 104.

Principal
G. Narayanamma Institute of Technology & Science (for woman)
Shaikpet, Hyderabad - 500 104.

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E-mail : principal@gnits.ac.in, Website : www.gnits.ac.in

Dt: 03-11-16
Hyderabad.

To
Dr.M.Satyam
Retd. Professor, IISC Bangalore
& Professor, Dept. of ECE,
Vasavi College of Engineering
Hyderabad.

Respected Sir,

G.Narayanamma Institute of Technology and Science(for women) whole heartedly appreciates your acceptance as **Chief guest** and delivering **Key note address** on 17/10/2016 for the one week workshop on "**Functional Approach to VLSI Design**" conducted in the Department of ECE from 17/10/2016 to 22/10/2016.

We are very happy to inform you that your lecture has been one of the very best. We thank you for your wonderful lecture and supporting us in knowledge sharing.

Wishing you all the best for future endeavors.

G. Narayanamma Institute of Technology & Science (For Women) Shaikpet, Hyd - 104.

With regards,

3/11/16

Dr.K.Ramesh Reddy,
Principal,
GNITS

Principal
G. Narayanamma Institute of
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E-mail : principal@gnits.ac.in, Website : www.gnits.ac.in

Dt: 03-11-16
Hyderabad.

To
Dr.K.Subbarangaiah,
Director, VedaIIT,
Hyderabad.

Respected Sir,

G.Narayanamma Institute of Technology and Science(for women) whole heartedly appreciates your acceptance as **Resource person** and delivering a lecture - **"FinFets-The promises and the challenges"** on 18/10/2016 for the one week workshop on "**Functional Approach to VLSI Design**" conducted in the Department of ECE from 17/10/2016 to 22/10/2016.

We are very happy to inform you that your lecture has been one of the best. We thank you for your wonderful lecture and supporting us in knowledge sharing.

Wishing you all the best for future endeavors.

With regards,

3/11/16

Dr.K.Ramesh Reddy,
Principal,
GNITS

G. Narayanamma Institute of Technology & Science for Women, Shaikpet, Hyd - 104.

Principal
G. Narayanamma Institute of Technology & Science (for woman)
Shaikpet, Hyderabad - 500 104.

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E-mail : principal@gnits.ac.in, Website : www.gnits.ac.in

Dt: 03-11-16
Hyderabad.

To
Mr.Raja Bandi,
Director,
Lucid VLSI,
Hyderabad .

Respected Sir,

G.Narayanamma Institute of Technology and Science(for women) whole heartedly appreciates your acceptance as **Resource person** and delivering a lecture - **"Introduction to System Verilog Assertions"** on 19/10/2016 for the one week workshop on **"Functional Approach to VLSI Design"** conducted in the Department of ECE from 17/10/2016 to 22/10/2016.

We are very happy to inform you that your lecture has been one of the best and got an excellent feedback. We thank you for your wonderful lecture and supporting us in knowledge sharing.

Wishing you all the best for future endeavors.

With regards,

3/11/16

Dr.K.Ramesh Reddy,
Principal,
GNITS

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Shaikpet, Hyderabad - 500 104.

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E-mail : principal@gnits.ac.in, Website : www.gnits.ac.in

Dt: 03-11-16
Hyderabad.

To
Usha Bandi
Staff Design Engineer,
Xilinx,Hyderabad .

Respected Madam,

G.Narayanamma Institute of Technology and Science(for women) whole heartedly appreciates your acceptance as **Resource person** and delivering a lecture - **"Introduction to VLSI Design Methodologies"** on 17/10/2016 for the one week workshop on **"Functional Approach to VLSI Design"** conducted in the Department of ECE from 17/10/2016 to 22/10/2016.

We are very happy to inform you that your lecture has been one of the best and got an excellent feedback. We thank you for your wonderful lecture and supporting us in knowledge sharing.

Wishing you all the best for future endeavors.

With regards,

Dr.K.Ramesh Reddy,
Principal,
GNITS

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E-mail : principal@gnits.ac.in, Website : www.gnits.ac.in

Dt: 03-11-16
Hyderabad.

To
Mr.Hirdesh Singal,
CEO, Seer Akademi
Hyderabad .

Respected Sir,

G.Narayanamma Institute of Technology and Science(for women) whole heartedly appreciates your acceptance as **Resource person** and delivering a lecture - **"Low power Integrated sensors for IOT"** on 17/10/2016 for the one week workshop on **"Functional Approach to VLSI Design"** conducted in the Department of ECE from 17/10/2016 to 22/10/2016.

We are very happy to inform you that your lecture has been one of the very best. We thank you for your wonderful lecture and supporting us in knowledge sharing.

Wishing you all the best for future endeavors.

With regards,

G. Narayanamma Institute of Technology & Science (for Women) ★ Shaikpet, Hyd - 104.

Dr.K.Ramesh Reddy,
Principal,
GNITS

Principal
G. Narayanamma Institute of
Technology & Science (for woman)
Shaikpet, Hyderabad - 500 104.

Important Dates:

Workshop dates: **17-10-2016 to 22-10-2016**

Last date for registration: **10-10-2016**

Registration Fee:

Academic Staff /Research Scholars/Delegates from Industry (non-IETE members): **Rs. 1,000/-**
(IETE members) : **Rs. 750/-**

PG students : **Rs. 500/-**

Address for Correspondence

Dr. K .Ragini,
Professor, Department of ECE,
GNITS, Hyderabad
Cell: 9849627161

M/s Deepthi Amuru
Asst. Professor, Department of ECE,
GNITS, Hyderabad
Cell: 9966437906
E-mail: workshopvlsi2016@gmail.com

For more details visit the website

www.gnits.ac.in

Chief Patron

Sri P Subba Reddy, Chairman

Patron

Smt G Srividya Reddy, Joint Secretary

Chairman

Dr.K.Ramesh Reddy, Principal

Convener

Dr.B.Venkateshulu, HOD ECE

Advisory Committee Member

Dr.P.V.D.Somasekhar Rao,Dean Academics

Organizing Committee

All Associate and Assistant Professors

of ECE Department

REGISTRATION FORM

1. Name of the Applicant:.....
   (Block Letters)
   .....
2. Gender: (M/F): .....
3. Educational Qualifications:.....
4. Designation:.....
5. Department: .....
6. Name of the Sponsoring Institute/Organization:
7. Signature/Seal of the Sponsoring Authority:
8. Address for Correspondence :
   (Including E-mail, Fax, Cell / Landline)
   .....
   .....
   .....
   .....
   .....
9. Is a member of IETE? **YES/NO**
   IETE Membership No. :
10. Is Accommodation required ? **YES / NO**
11. Demand Draft Amount: Rs:
    Demand Draft No:.....
    Bank:.....
    Dated:.....

Signature of the Applicant with date

A One Week Workshop on

"Functional Approach to VLSI Design"

(17-10-16 to 22-10-16)

Organized by

DEPT. OF ECE
G. NARAYANAMMA INSTITUTE OF TECHNOLOGY & SCIENCE (FOR WOMEN)
ISO 9001:2008 Certified, NAAC Accredited
Shaikpet, Hyderabad, T.S.

In Collaboration with

सह वीर्यं करवावहै
Institution of Electronics & Telecommunication Engineers
IETE, Hyderabad Chapter
and
CoreEL Technologies
Enabling Excellence
Core EL Technologies, Hyderabad

Coordinators

Dr.G.Laxmi Narayana,
Chairman, IETE, Hyderabad chapter

Dr.K.Ragini,
Professor, ECE Dept., GNITS

M/s.Deepthi Amuru,
Assistant Professor, ECE Dept., GNITS

ABOUT GNITS:

G. Narayanamma Institute of Technology & Science (for Women), was founded by Late Sri G. Pulla Reddy garu in 1997, with the objective of providing an excellent learning facility for women to pursue education in engineering and the institute aims to promote Technical Education among women to enhance and build-up a new generation of thinkers, innovators and planners in the technical realms of Science & Technology. It is today considered one of the best engineering colleges in Hyderabad. GNITS is affiliated to Jawaharlal Nehru Technological University Hyderabad (JNTUH), accredited by NAAC and is approved by All India Council for Technical Education (AICTE).

GNITS has recorded phenomenal growth in a short span of time. The college has five undergraduate programs in ECE, ETM, EEE, CSE, IT. In addition to UG, PG Programs in DECE, PEED, CSE, WMC and CNIS are offered.

ABOUT ECE DEPARTMENT:

ECE Department was started in 1997 with an intake of 60 and in a short period, the intake was increased to 180.Department has conducted many state level short-term courses in Digital Image Processing , DSP, VLSI, Microprocessors & Micro controllers and paper presentations under IETE, ISTE and ECE associations. The department has well established labs, with state of art equipment like trainer kits such as DQPSK QAM, trellis coder and conv. encoder and decoder, FHSS software & advanced softwares like Active HDL, XILINX, Mentor Graphics tool in ECAD/VLSI lab, MATLAB, Multisim, P-Spice & KEIL. The department has highest student placements and Awards.

Eligibility:

Faculty of Educational Institutions/ Research Scholars/ Persons working in R& D Organization/ PG students, in Electronics & Communication/ Electrical/ Computer Science and allied branches of Engineering, are eligible to apply.

IETE Hyderabad Centre

IETE Hyderabad Centre started on 11th September, 1973 has completed 40 years and is growing up. It was declared as Best Centre Best Local Centre in India during the years 1992-93, 1994-95, 1995-96, 1996-97, 1999-2000, Best Performance Centre Award for the year 2003 – 2004 and 2nd Best Centre for the year 2012-2013. The IETE Hyderabad Centre has Corporate and Student Members. Hyderabad Centre has proudly undertaken to organize the Zonal Seminar-cum-National Symposium on 29th & 30th March, 2014.

CoreEL Technologies

CoreEL Technologies is a Customer Application Specific Product & Solutions (CASPS) company offering innovative solutions, which ranges across Intellectual Property (IP) cores, Design & Development, Bespoke System Design & Prototype Development, Next-Gen Digital products, Integrated solutions, Low Volume Manufacturing, System Upgrades and Obsolescence management, EDA tools, COTS products, Semiconductor solutions and Technology Training. CoreEL is a leading developer of advanced electronic system level products

About the Workshop:

VLSI Design has become an important domain in the field of Digital and Analog circuits. The aim of the course is to provide a basic knowledge on advanced design concepts in VLSI Design and motivate the faculty/students towards research in the field of VLSI. This workshop provides the knowledge on system Verilog, different techniques for Low Power Design, basics on Analog and mixed signal design and also provides hands on experience using Xilinx Zynq boards and mentor graphics for backend circuit design.

COURSE CONTENT:

- Review of VLSI design methodologies
- Introduction to System Verilog Assertions
- Design promises and challenges for digital circuit design using FinFETs.
- Analog and mixed signal design flow
- Techniques for low power design and ultra-low power circuits
- Low power Integrated sensors for IOT
- Lab sessions using Xilinx Zynq board on Data motion networks and accelerators
- Lab sessions using mentor graphics on Semi-custom VLSI circuit backend design

Resource Persons:

1. Dr. G.Laxmi Narayana, Chairman, IETE Hyderabad chapter
2. Dr. M.Satyam, Retd. Professor, IISC, Bangalore
3. Dr. K. Lal Kishore, Former vice chancellor, JNTUA
4. Dr. M.Madhavi Latha, JNTUH
5. Dr. P.A.Govindacharyulu, Vasavi Engineering College
6. Dr. K.Subbarangaiah,, Director, Veda IIT
7. Mr.Hirdesh Singal, Seer Akademi

Other resource Persons are drawn from industries such as – DRDL, AMD, Xilinx and LUCID VLSI.

How to Apply:

Interested persons may apply in the prescribed format along with the Registration fee. Payments should be made through a Demand Draft drawn in favor of **"The Principal, G Narayanamma Inst. of Technology & Science for Women** payable at Hyderabad or by cash at the time of registration. The registration form can be downloaded from www.gnits.ac.in. The duly filled registration form along with scanned copy of the DD has to be sent to **workshopvlsi2016@gmail.com** on or before **10th October '2016.** The DD must also be submitted at GNITS during registration. The participants are advised to register well in advance of the scheduled dates.

Accommodation:

Working lunch and snacks will be provided for all the participants and limited accommodation would be provided free of cost to the ladies.

5

WEEK WORKSHOP ON "FUNCTIONAL APPROACH TO VLSI DESIGN"

(17.10.2016-22.10.2016)

G. Narayanamma Institute of Technology & Science,

Shaikpet, Hyderabad – 500008

Agenda:

Review of VLSI design methodologies

Introduction to system Verilog assertions

Design promises and challenges for digital circuit design using FinFETs

Analog and mixed signal design flow

Techniques for low power design and ultra low power circuits

Low power integrated sensors for IOT

Lab sessions using Xilinx Zynq board on Data motion networks and accelerators

Lab sessions using Mentor graphicson semi custom VLSI circuit backend design

Day1:

Session 1:

Dr.M.Satyam sir, Retd Professor, IISC, Bangalore spoke about "FUNCTIONAL APPROACH TO VLSI DESIGN". He taught about the different approaches to integration and miniaturization. Before entering into the actual topic he had explained the evolution of VLSI, and then the constraints and features of different approaches, the hierarchical approach to Functional design.

Session 2:

Dr.G.Laxmi Narayana, Chairman, IETE, Hyderabad.

His topic was "FREQUENCY CONSIDERATION FOR CHIP DESIGN". He explained about the pre requisites for chip design, and spoke about the history of electronics and technology requirement. Under the technology requirement he explained in detail about the fabrication technology, semiconductors and doping and basic design methodology, VHDL Hierarchy, Various interconnect such as metal interconnect, copper interconnect. And finally he explained about the frequency consideration for VLSI Chip design.

Session 3:

Mrs. B.Usha, design engineer from Xilinx spoke about "VLSI Design Methodologies".

She explained in detail about Front end and back end VLSi design flow. She included many more subtopics in design flow. She shared her experience in attending the Embedded system conference 2016. She suggested how to overcome the gap between the industry and academics. Faculty should become the bridge between these two. She explained the importance of IOT and its application areas.

Session 4:

Mr.Hirdesh Singal, CEO, Seer Akademi sopke about "Low power Integraetd sensors for IOT".

From Core El Technologies given an Overview of SDSoC design flow and Zynq architechture, Data motion networks

Session 3:

Lab session participants understood the importance of creating hardware accelerators, Pragmas and data motion networks

Day 5:

Session 1:

Sharath from Core EL technologies explained explained "FPGA Architecture", ASIC and FPGA design flow and its comparisons. He explained the differenece between Full custom design and semi custom design tool.

Session 2:

N.S.Murthy, professor from Vasavi college of engineering spoke about "System Level power optimization".

He concentrated on explaining the need of low power and how to obtain it in various stages of design flow.

Session 3:

Participants generated a circuit layout, DRC, Design verification and simulation using mentor graphics.

Day 6:

Participants were Familiarized with Semi-custom design tools to generate circuit layout, DRC, Design verification and simulation.

The major focus of the workshop is to upgrade the research skills of teachers, especially those teachers who have not had an opportunity to acquaint themselves with recent developments in research methods .The workshop was a grand success with total participants of 44.Among this ,23 faculty are from different colleges,10 faculty from GNITS, and 11 PG students from other colleges like TKRCET-9,Osmania university -1 NMREC-1.The valedictory function was held on 22-10-16 and certificates were issued for all participants.

K. Ragini 23/10/16

Dr.K.Ragini

Workshop Coordinator

One Week Workshop on "Functional Approach to VLSI Design"
(17-10-2016 to 22-10-2016)

S.No/Date	9.30 AM to 11.00AM		11.15 AM to 12.45 PM		1.45 PM to 3.15 PM	3.30 PM to 5.00 PM
17-10-2016	Registration & Inaugural Session	Keynote Address	Introduction to VLSI design Methodologies		Introduction to System Verilog Assertions	
		Dr. M. Satyam Retd.Professor, IISC.Bangalore	Dr. M.Madhavi Latha. Professor,JNTUH		Mr. Raja Bandi. Director. Lucid VLSI	
18-10-2016	FinFets-The promises and the chanllenges		RFCMOS design	LUNCH	7-Series FPGA Architecture	
	Dr.K.Subbarangaiah. Director. VedaIIT		Mrs.Nalini, DRDL		Mr.Mukesh Director. Technolexes	
19-10-2016	A lecture on "Analog Mixed signal design flow		Techniques for Low Power Design		Low power Integrated sensors for IOT	Leakage and Power Reduction at Architecture Level
	Dr.Govindacharyulu, Professor. Vasavi Engg. College		Dr.Lal Kishore .Former vice-chancellor.JNTUA		Mr.Hirdesh Singal. Seer Akademi	Mr.J.Kiran Kumar. Xilinx
20-10-2016	Overview on SDSoC design flow and Zynq AP SOC Architecture		Data motion networks	BREAK	Lab session on VLSI Circuit design using Pragmas and data motion networks	Lab session on Profiling application and create accelerators
	Core EL Technologies		Core EL Technologies		Core EL Technologies	Core EL Technologies
21-10-2016	Ultra Low power Subthreshold digital circuits		Full custom design tools to generate circuit layout. DRC. Design verification and simulation		Lab session on Full custom design tools to generate circuit layout. DRC. Design verification and simulation	Lab session on Full custom design tools to generate circuit layout. DRC. Design verification and simulation
	Dr.K.Ragini. GNITS		Core EL Technologies		Core EL Technologies	Core EL Technologies
22-10-2016	Semi custom design tools to generate circuit layout. DRC. Design verification and simulation		Lab session on Semi custom design tools to generate circuit layout. DRC. Design verification and simulation		Lab session on Semi custom design tools to generate circuit layout. DRC. Design verification and simulation	Valedictory Session
	Core EL Technologies		Core EL Technologies		Core EL Technologies	

Coordinators

1. **Dr.K.Ragini,** K.Ragini
Professor, ECE, GNITS

2. **A.Deepthi** D.Y
Asst.Professor, ECE, GNITS

Dr.B.Venkateshulu 7/9/16
HOD,ECE

G.Narayanamma institute of Technology & Science (for women)

Department of Electronics & Communication Engineering

One Week Workshop on "Functional Approach to VLSI Design"

(17-10-2016 to 22-10-2016)

सद वीर्य करवावहै
Institution of Electronics & Telecommunication Engineers

Core EL technologies
Enabling Excellence

Chief Patron
Sri P. Subba Reddy, Chairman

Patron
Smt G. Srividya Reddy, Joint Secretary

Chairman
Dr.K.Ramesh Reddy, Principal

Convener
Dr.B.Venkateshulu, HOD ECE

Advisory Committee Member
Dr.P.V.D.Somasekhar Rao, Dean Academics

Coordinators
Dr.G.Laxmi Narayana, Chairman, IETE, Hyderabad chapter

Dr.K.Ragini, Professor, ECE Dept., GNITS

M/s.Deepthi Amuru, Assistant Professor, ECE Dept., GNITS

Organizing Committee
All Associate and Assistant Professors of ECE Department

S.No/Date	9.45 AM to 11:00AM	11.15 AM to 12.30 PM		1.45 PM to 3.00 PM	3.15 PM to 4.30 PM
17-10-2016	Registration & Inaugural Session	Keynote Address	Frequency consideration for chip design	Introduction to VLSI Design Methodologies	Low power Integrated sensors for IOT
		Dr. M. Satyam Retd.Professor, IISC,Bangalore	Dr.G.Laxmi Narayana, IETE Chairman,Hyderabad Principal, Anurag group of Institutions	Mrs.B.Usha, Staff Design Engineer Xilinx	Mr.Hirdesh Singal, CEO, Seer Akademi
18-10-2016	FinFets-The promises and the challenges		Techniques for Low Power Design	Introduction to Power Aware Verification: A step towards keeping up with the low power trends.	
	Dr.K.Subbarangaiah, Director, VedaIIT		Dr.N.Siva Shankar Reddy, Assoc.Professor, Vasavi College of Engg.	Rakshith Rangaswamaiah Application Engineer Functional Verification, Mentor Graphics	
19-10-2016	Ultra Low power Subthreshold digital circuits"		A lecture on "Analog Mixed signal design flow	Introduction to System Verilog Assertions	
	Dr.K.Ragini, Professor, GNITS		Dr.P.A.Govindacharyulu, Professor, Vasavi College of Engg.	Mr. Raja Bandi, Director, Lucid VLSI	
20-10-2016	Overview on SDSoC design flow and Zynq AP SOC Architecture		Data motion networks	Lab session on VLSI Circuit design using Pragmas and data motion networks	Lab session on Profiling application and create accelerators
	Core EL Technologies		Core EL Technologies	Core EL Technologies	Core EL Technologies
21-10-2016	Full custom design tools to generate circuit layout, DRC, Design verification and simulation		System level power optimization	Lab session on Full custom design tools to generate circuit layout, DRC, Design verification and simulation	Lab session on Full custom design tools to generate circuit layout, DRC, Design verification and simulation
	Core EL Technologies		N.S.Murthy, Professor Vasavi college of Engineering	Core EL Technologies	Core EL Technologies
22-10-2016	Semi custom design tools to generate circuit layout, DRC, Design verification and simulation		Lab session on Semi custom design tools to generate circuit layout, DRC, Design verification and simulation	Lab session on Semi custom design tools to generate circuit layout, DRC, Design verification and simulation	Valedictory Session
	Core EL Technologies		Core EL Technologies	Core EL Technologies	

LUNCH BREAK

Coordinators

1. **Dr.K.Ragini, Professor, ECE, GNITS**

2. **A.Deepthi Asst.Professor, ECE, GNITS**

Dr.B.Venkateshulu HOD,ECE

15/10/16

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☎ : 040-23566803
040-23565648
Fax: 040-23564187

ed Institution

G. NARAYANAMMA INSTITUTE OF TECHNOLOGY & SCIENCE

Accredited by NAAC of UGC upto 20-02-2019 **(For Women)**
(Sponsored by G. Pulla Reddy Charities Trust, Hyderabad.)
(Accredited by NBA (from May 2007 to April 2010) Approved by AICTE & Affiliated to J N T U - H)
8-1-297/2/I, Shaikpet, Hyderabad - 500 008. T.S. INDIA
E-mail : principalgnits97@gmail.com, Website : www.gnits.ac.in

Date:12/09/2016

To

Respected Principal/Sir/Madam,

Subject: One Week workshop on **"Functional Approach to VLSI Design" being organized during 17th Oct to 22nd Oct 2016 at GNITS jointly with IETE,** Hyderabad chapter – Regarding.

We take pleasure to inform you that ECE dept. is organizing one week workshop on **"Functional Approach to VLSI Design"** to provide an opportunity for faculty members to improve their research and technical skills in the domain of VLSI.

In this context we have immense pleasure in inviting your faculty to participate in the workshop with great zeal and enthusiasm. An informative brochure is attached for your kind perusal. It is requested that the same may please be prominently displayed on the notice boards of your institution for wide and effective publicity. Applicants may look for more details at *www.gnits.ac.in* and also can download the registration form from the college website.

Thanking You.

With Regards

12/9/16

Dr.K.Ramesh Reddy
Principal,
GNITS

Principal
G. Narayanamma Institute of Technology & Science (for women)
Shaikpet, Hyderabad - 500 104.

FACULTY

One Week Workshop on "Functional Approach to VLSI Design"

List of Participants

S No.	Name	Designation	Dept.	College	Mobile	Mail ID	IETE Membership No. (If Any)	DD No.	Amount	Sign
1	Mr FACHA JETHAN	Ast. Professor	ECE	SLVCET,	9502925678	jethan_ec@yahoo.in	NA.		1000/-	
2	G. Mahesh Kumar	Asst. Prof	ECE	NMREC	9849378059	mahesh.kumar.ece@nmrec.edu.in	—		1000/-	
3	K. Satish	Asst. Prof	ECE	TKRCET	9676289345	satish.kunapareddy@live.in	—		1000/-	
4	K. Ramakrishnareddy	Assoc. Prof	ECE	TKRCET	9951527480	krishna222@gmail.com	—		1000/-	
5	P. kalyani	Asst Prof	ECE	TKRCET	9989648497	kalyani_vpk@yahoo.co	—		1000/-	
6	ATHIRA G. KRISHNAN	Sr. Asst. Prof	ECE	CVRCE	9490166503	athira_rashad@yahoo.co.in	No	954316	1000/-	
7	S. Swetha	Asst. Prof	ECE	CVRCE	9.38610.3267	swetha.sillveri@gmail.com	NO		1000/-	
8	G. Snehalatha	Asst prof	ECE	CVRCE	9397654772	Snehamj401@gmail.com	NO	—	1000/-	
9	M.V. Sushumna	Asst Prof.	ECE	CVRCE	8008854880	sushumna451@gmail.com	NO	—	1000/-	
10	P. Padma	Asst. prof	ECE	G.E.C.	9985846039	Padma.dandyala@gmail.com	NO		1000/-	
11	K V Gowreesrinivas	Research Scholar	ECE	PU	9440155583	Srinu4336@gmail.com	NO		1000/-	
12	Y Bhavani prasad	Asst prof	ECE	GEC	8125125729	bhavaniprasad.ece@gmail.com	No	164213	1000/-	
13	H. Thanmaya Babu	Asst prof	ECE	GEC	8143800990	Phani.nitis@gmail.com	No	164212	1000/-	
14	V. Radha Krishna	"	ECE	GNITS	9849071869	collevirk@yahoo.com	YES		750/-	
15	B. Narmada Reddi	Asst. Prof	ECE	GNITS	9490215917	bnarmadareddi@gmail.com	No		due.	
16	N. LAKSHMI	Asst-Prof	ECE	GNITS	7032676124	laxmimittra@gmail.com	No		1000/-	
17	MD. ZAKIR HUSSAIN	Asst. prof	ECE	MTCET	8686429678	zakirhussain@ieee.org	NO		1000/-	
18	P A Pravallika	Asst prof	ECE	BRECW	9618144449	Sravanthi.avvaru@gmail.com	yes	049602	750/-	
19	Nikhat Parveen	Asst Prof	ECE	BRECW	9949959059	nikhatparveen2@gmail.com	NO	048959	1000/-	
20	P. Roopa Ranjani	Asst. Prof	ECE	GNITS	9703414326	roopa.ece@gmail.com	No	—	1000/-	
21	S. Prashanthi	Asst. Prof	ECE	BRECW	9949241445	shanthik2005@rediffmail.com	yes	049601	750/-	
22	D. Sreelatha Raj	Asst. prof.	ECE	GPCET	7036109455	greeen.shwetharaj@gmail.com	-	049181	1000/-	
23	G. SUNITHA	Asst. Prof	ETM	GNITS	9959966461	sunitha.tappari@gmail.com	NO	[illegible]	1000/-	
24	S.V. Jaya Bhargavi	Asso. Prof	ECE	SVCET	9704688538	bhargavi.svpudi@gmail.com	NO	—	1000/-	
25	Premalatha	Asso. Prof	ECE	SVCET	9848288785	Premalatha.katikela@yahoo.com	NO	—	1000/-	
26	G. NEHA	Asst. prof	ECE	AARM	9391507312	Sneha.223039@yahoo.com	NO	—	1000/-	
27	T. SIVAPRASAD	Asst. Prof	ECE	AARM	9030388914	sivaprasad007@gmail.com	NO	—	1000/-	
28	B. Ravichandra Rao	Asst. Prof	EEE	GNITS	9901649055	rao.ravichandra@gmail.com	NO	—	1000/-	
29	V. Rakesh kumar	Asst. prof	ECE	GNITS	7207525875	rakesh.yacharam@gmail.com	No.	—	due.	
30	T. Ramasri	Asst-prof	ECE	GNITS	8801706536	ramasri.thallo@gmail.com	NO	—	1000/-	

bhargavi.sapuri2011@gmail.com

Premalatha.katikela@yahoo.com

S No.	Name	Designation	Dept.	College	Mobile	Mail ID	IETE Membership No. (If Any)	DD No.	Amount	Sign
31	M. Shanthi	Asst Prof	ECE	GNITS	9177687116	shanthi3011@gmail.com	No.	—	500/-	
32	N. Hasini	Aut. Prof	ECE	GNITS	9849712935	hasini.n@yahoo.in	NO	—	500/-	
33	K. Sireesha Rao	Aut. Prof	ECE	GNITS	9966564633	Sireesha.Praj1@gmail.com	NO	—	500/-	
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STUDENTS

One Week Workshop on "Functional Approach to VLSI Design"

List of Participants

S No.	Name	Dept.	College	Mobile	Mail ID	DD No.	Amount	Sign
1	G. Praveen.	ECE	UCE, OU	9989286048	08601A0439@gmail.com		500/-	
2	T. Sadhana	ECE	TKRCET	8464049355	sadhanathuedimilla@gmail		500/	
3	A. Shankaraiah	ECE	TKRCET	9290412222	shankaraiah29@gmail.com		500/-	A. Shankaraiah
4	Sagarika	ECE	TKRCET				500/	
5	M. Teja	ECE	TKRCET	9603881569	mizyalateja@gmail.com		500/-	Teja
R 6	K. Soujana	ECE	TKRCET	7801042639	soujanakanaka27@gmail.com		500/-	Soujana
~~X 7~~	~~A. Divyasree~~	~~ECE~~	TKRCET	8331933751			500/-	Divyasree
R 8	S. Pattabi Reddy	ECE	TKRCET	9959275758	pattusekharreddy@gmail		500/-	
X 9	~~U. Sandeepyadav~~	~~ECE~~	~~TKRCET~~				500/-	
R 10	B. Soumya Sree	ECE	TKRCET	7893029904	bollipogu.soumyasree94@gmail		500/-	
11	~~A. Divya Sree~~	ECE	TKRCET	8331933751	divya.sree1029@gmail.com		500/-	
12	G. Sandeep Yadav	ECE	TKRCET	9866383677	sandeep3648@gmail.com		500/-	G. Yadav
13.	V. Krishna Kishore	ECE	NMREC	8886455513	krishnakishore.ece@gmail.com		500/-	
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Important Dates:

Workshop dates: **17-10-2016 to 22-10-2016**

Last date for registration: **10-10-2016**

Registration Fee:

Academic Staff /Research Scholars/Delegates from Industry (non-IETE members): **Rs. 1,000/-**
(IETE members) : **Rs. 750/-**

PG students : **Rs. 500/-**

Address for Correspondence

Dr. K. Ragini,
Professor, Department of ECE,
GNITS, Hyderabad
Cell: 9849627161

M/s Deepthi Amuru
Asst. Professor, Department of ECE,
GNITS, Hyderabad
Cell: 9966437906
E-mail: workshopvlsi2016@gmail.com

For more details visit the website

www.gnits.ac.in

Chief Patron

Sri P Subba Reddy, Chairman

Patron

Smt G Srividya Reddy, Joint Secretary

Chairman

Dr.K.Ramesh Reddy, Principal

Convener

Dr.B.Venkateshulu, HOD ECE

Advisory Committee Member

Dr.P.V.D.Somasekhar Rao,Dean Academics

Organizing Committee

All Associate and Assistant Professors

of ECE Department

REGISTRATION FORM

1. Name of the Applicant: KUNA SATEESH
   (Block Letters)
2. Gender: (M/F): M
3. Educational Qualifications: M.Tech
4. Designation: Assistant Professor
5. Department: E C E
6. Name of the Sponsoring Institute/Organization:
   TKR COLLEGE OF ENGG. & TECHNOLOGY
7. Signature/Seal of the Sponsoring Authority:
   Dr.D.V. Ravi Shankar
   M.Tech.,Ph.D.
   PRINCIPAL
   TKR College of Engineering & Technology
   Medbowli, Meerpet, Hyderabad.
8. Address for Correspondence:
   (Including E-mail, Fax, Cell / Landline)
   H.NO: 14-202/6, RN Reddy Nagar, Meerpet, HYD.
   9703282548
9. Is a member of IETE? YES/NO
   IETE Membership No. :
10. Is Accommodation required ? YES / NO
11. Demand Draft Amount: Rs:
    Demand Draft No:.....
    Bank:.....
    Dated:.....

Signature of the Applicant with date

A One Week Workshop on

"Functional Approach to VLSI Design"

(17-10-16 to 22-10-16)

Organized by

DEPT. OF ECE
G. NARAYANAMMA INSTITUTE OF TECHNOLOGY & SCIENCE (FOR WOMEN)
ISO 9001:2008 Certified, NAAC Accredited
Shaikpet, Hyderabad, T.S.

In Collaboration with

सह बोधं कल्याणे
Institution of Electronics & Telecommunication Engineers
IETE, Hyderabad Chapter
and
Core EL technologies
Enabling Excellence
Core EL Technologies, Hyderabad

Coordinators

Dr.G.Laxmi Narayana,
Chairman, IETE, Hyderabad chapter

Dr.K.Ragini,
Professor, ECE Dept., GNITS

M/s.Deepthi Amuru,
Assistant Professor, ECE Dept., GNITS

G.Narayanamma institute of Technology & Science (for women)
Department of Electronics & Communication Engineering
One Week Workshop on "Functional Approach to VLSI Design"
(17-10-2016 to 22-10-2016)

Institution of Electronics & Telecommunication Engineers

CoreEL Technologies
Enabling Excellence

Name:

FEEDBACK FROM PARTICIPANTS

College Address:

Date & Time	Name of the Resource person	Topics	Presentation/Content			Any other Remarks
			Below Average	Good	Excellent	
17-10-2016	Dr. M. Satyam Retd.Professor, IISC,Bangalore	Keynote Address		✓		Not audible at that time.
17-10-2016 (11.15 AM to 12.30 PM)	Dr.G.Laxmi Narayana, IETE Chairman,Hyderabad Principal, Anurag group of Institutions	Frequency consideration for chip design			✓	
17-10-2016 (1.45 PM to 3.00 PM)	Mrs.B.Usha, Xilinx	Introduction to VLSI Design Methodologies		✓		
17-10-2016 (3.15 PM to 4.30 PM)	Mr.Hirdesh Singal Seer Akademi	Low power Integrated sensors for IOT		✓		
18-10-2016 (9.45 AM to 11:00AM)	Dr.K.Subbarangaiah Director, VedaIIT	FinFets-The promises and the challenges			✓	
18-10-2016 (11.15 AM to 12.30 PM)	Dr.N.Siva Shankar Reddy, Assoc.Professor, Vasavi College of Engg.	Techniques for Low Power Design			✓	
18-10-2016 (1.45 PM to 4.30 PM)	Rakshith Rangaswamaiah Application Engineer Functional Verification, Mentor Graphics	Introduction to Power Aware Verification: A step towards keeping up with the low power trends.			✓	

Valuable Suggestions:

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25-10-2016

To
The Principal,
GNITS,
Shaikpet,
Hyderabad-08.

// Through proper channel //

Sub: Submission of statement of expenditure for **One week workshop on "Functional Approach to VLSI"** during 17-10-2016 to 22-10-2016. Regd...

Respected sir,

I, Dr.K.Ragini, Professor and Mrs.A.Deepthi, Asst. Prof., of ECE department have planned and organized an One week workshop on "Functional Approach to VLSI Design" during 17-10-2016 to 22-10-2016 in collaboration with IETE, Hyderabad chapter. We are here by submitting the statement of expenditure along with bills enclosed.

Thanking you sir,

Yours faithfully,

K. Ragini

Dr.K.Ragini,

Professor, Dept. of ECE.

Mrs. A. Deepthi,

Asst.Prof., Dept. of ECE.

G. NARAYANAMMA INSTITUTE OF TECHNOLOGY AND SCIENCE

सह वीयं करवावहै
Institution of Electronics & Telecommunication Engineers

One Week Workshop on "Functional Approach to VLSI Design"

(17-10-16 to 22-10-16)
In collaboration with
IETE, Hyderabad chapter

Statement of Expenditure towards Honorarium & Transportation of Resource Persons

Sl.No	Particulars	Amount (Rs.)
Honorarium to Resource Persons		
1.	Dr. M. Satyam Retd. Prof, IISC Bangalore. Professor, Vasavi College of Engineering, Hyderabad.	3000.00
2.	Dr.G.Laxmi Narayana Chairman, IETE, Hyderabad Chapter. Principal, Anurag College of Engineering, Hyderabad.	3000.00
3.	Mrs.B.Usha Staff Design Engineer, Xilinx Pvt. Ltd., Hyderabad	3000.00
4.	Dr.HirdeshSinghal CEO, Seer Akademi, Hyderabad	3000.00
5.	Dr.K.Subbarangaiah Director, VedaIIT, Hyderabad	3000.00
6.	Dr.N.Siva Shankar Reddy Assoc.Prof., Vasavi College of Engineering, Hyderabad	3500.00
7.	Mr.RajaBandi Director, Lucid VLSI, Hyderabad	6000.00
8.	Dr.P.A.Govindacharyulu, Professor, Vasavi College of Engineering, Hyderabad	3500.00
9.	Dr.N.S.Murthy Professor, Vasavi College of Engineering, Hyderabad	3000.00
Transportation to Resource Persons		
10.	M/s. Ola/Uber Travels, Hyderabad	2400.00
	Total:	**33400.00**

Income and Expenditure statement

25-10-2016

Income and Expenditure statement of the One week workshop on **"Functional Approach to VLSI Design"** during 17th October to 22nd October, 2016.

Sl.No.	Particular	Amount (Rs.)
1.	Advance Amount take from College	54,000 /-
2.	Amount collected from participants (deposited at office)	36,500 /-
	Total amount credited	90,500 /-

Amount Spent:

Sl.No.	Particulars	Amount (Rs.)
1.	Honorarium	31000
2.	Transport	2400
3.	Canteen	26500
4.	Banners	800
5.	Certificates	1000
6.	Stationary(folders)	1485
7.	Postal Charges	950
8.	Shawls + Bouquets+ Sweet Packets	1760
9.	Decoration for inaugural	200
10.	Miscellaneous	2265
	Total amount spent	68,360 /-

Balance amount need to be sanctioned=68360 – 54000 = Rs.**14360** /-

Final balance amount left after the conduction of workshop:

90500 – 68360 = Rs. **22,140** /-

Enclosed: 1. Sanction letter

2. Bills

54,000
36,500
17,700

K. Ragini

Dr.K.Ragini,
Professor, Dept. of ECE.

D. Deepthi

Mrs. A. Deepthi
Asst.Prof., Dept. of ECE

Date: 06-09-16

Budget Estimation for One week workshop on "Functional Approach to VLSI Design"

(17-10-2016 to 22-10-2016)

The following are the details of budget estimate for one-week workshop –Regd.

1.	Honorarium for Resource persons (Rs. 3000 per session, 12*3000)	Rs. 36,000	
2.	Transportation for Resource persons (1000 * 12)	Rs. 12,000	
3.	Working Lunch (expecting 30 participants, 6*90*40)	Rs. 21,600	
4.	Amount to be collected from participants(Rs.1000 for non-IETE members) and (Rs.750 for IETE members) (1000*20+750*10 approx.)		Rs. 27,500
5.	Stationary for the Participants	Rs. 800	
6.	Brochure and Postal charges	Rs.5600	
7.	Certificates	Rs.500	
8.	Miscellaneous	Rs.5000	
		Rs.81,500	Rs. 27,500
	Total estimated expenditure	Rs. 54,000	

Approximately budget of Rs. 54,000 is the estimate for the one week workshop.

Sincerely.

K. Ragini

Dr. K.Ragini
Course Coordinator

Deepthi Amuru

Co-Course Coordinator

Dr.B.Venkateshulu

HOD, ECE

G. Narayanamma Institute of Technology & Science,

Shaikpet, Hyderabad – 500008

Academic Year-2016-17

REPORT OF ONE WEEK WORKSHOP ON

"FUNCTIONAL APPROACH TO VLSI DESIGN"

(17.10.2016-22.10.2016)

A one week Workshop on "Functional Approach to VLSI Design "is organized by Department of ECE in COLLABORATION with IETE,Hyderabad Chapter and Core EL Technologies,Hyderabad from 17-10-16 to 22-10-16.The coordinators for the workshop are Dr.K.Ragin,Professor ECE Department and Mrs.Deepthi Amuru,Assistant Professor,Department of ECE.

VLSI Design has become an important domain in the field of Digital and Analog circuits. The aim of the course is to provide a basic knowledge on advanced design concepts in VLSI Design and motivate the faculty/students towards research in the field of VLSI. This workshop provides the knowledge on system Verilog, different techniques for Low Power Design, basics on Analog and mixed signal design and also provides hands on experience using Xilinx Zynq boards and mentor graphics for backend circuit design. The major focus of the workshop is to upgrade the research skills of teachers, especially those teachers who have not had an opportunity to acquaint themselves with recent developments in research methods .The workshop was a grand success with total participants of 44.Among this ,23 faculty are from different colleges,10 faculty from GNITS, and 11 PG students from other colleges like TKRCET-9,Osmania university -1 NMREC-1.The valedictory function was held on 22-10-16 and certificates were issued for all participants.

The following topics were discussed in the workshop.

- Introduction to system Verilog assertions
- Design promises and challenges for digital circuit design using FinFETs
- Analog and mixed signal design flow
- Techniques for low power design and ultra low power circuits
- Low power integrated sensors for IOT
- Lab sessions using Xilinx Zynq board on Data motion networks and accelerators
- Lab sessions using Mentor graphics on semi custom VLSI circuit backend design

Co-Ordinator

Dr.K.Ragini