DEPT. OF ELECTRONICS & COMMUNICATION ENGG

CERTIFICATE

THIS IS TO CERTIFY THAT THE MAJOR PROJECT ENTITLED

LOW POWER 4×4 BIT MULTIPLIER DESIGN USING DADDA ALGORITHM

IS THE BONAFIDE WORK OF

Ch.K.J. Poojitha	16251A0409
Vadloori Pavani	17255A0404
Gulle Geetha Sree	16251A0417
Sapavat Manjula	16251A0448

SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIREMENT FOR THE AWARD OF DEGREE OF BACHELOR OF TECHNOLOGY IN ELECTRONICS AND COMMUNICATION ENGINEERING DURING THE YEAR 2018-2019

Dr.B.Venkateshulu
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