DEPT. OF ELECTRONICS & COMMUNICATION ENGG

CERTIFICATE

THIS IS TO CERTIFY THAT THE MAJOR PROJECT ENTITLED

NOVEL HIGH SPEED VEDIC MULTIPLIER PROPOSAL INCORPORATING ADDER BASED ON QUATENERY SIGNED DIGIT NUMBER SYSTEM

IS THE BONAFIDE WORK OF

S. Apurva	16251A0447
G. Maneesha	16251A0412
Y. T. Tejasa	16251A0460
S Prathyusha	16251A0452

SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIREMENT FOR THE AWARD OF DEGREE OF BACHELOR OF TECHNOLOGY IN ELECTRONICS AND COMMUNICATION ENGINEERING DURING THE YEAR 2018-2019

10/9/20

Dr.B.Venkateshulu

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GUIDE