DEPT. OF ELECTRONICS & COMMUNICATION ENGG

CERTIFICATE

THIS IS TO CERTIFY THAT THE PROJECT ENTITLED

ESTIMATION OF POWER AND DELAY OF 4-BIT ARITHMETIC AND LOGIC UNIT IS THE BONAFIDE WORK OF

B.Shivani

(18251D3802)

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENT FOR THE AWARD OF DEGREE OF MASTER OF TECHNOLOGY IN DIGITAL ELECTRONICS AND COMMUNICATION ENGINEERING DURING THE ACADEMIC YEAR 2018-2019.

HOD OF ECE DEPT
Dr. B. VENKATESHULU

INTERNAL GUIDE
V.Shankar