

DEPT. OF ELECTRONICS & COMMUNICATION ENGG

CERTIFICATE

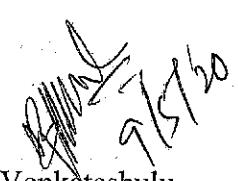
THIS IS TO CERTIFY THAT THE MAJOR PROJECT ENTITLED

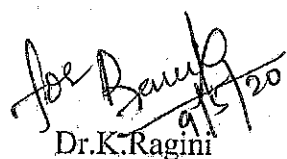
**LOW POWER 4×4 BIT MULTIPLIER DESIGN USING DADDA
ALGORITHM**

IS THE BONAFIDE WORK OF

| | |
|--------------------|------------|
| Rasamalla Anusha | 16251A04G3 |
| Goli Yaminisadhana | 17255A0426 |
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SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIREMENT FOR THE AWARD
OF DEGREE OF BACHELOR OF TECHNOLOGY IN ELECTRONICS AND
COMMUNICATION ENGINEERING DURING THE YEAR 2019-2020


Dr.B.Venkateshulu
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GUIDE