DEPT. OF ELECTRONICS & COMMUNICATION ENGG

CERTIFICATE

THIS IS TO CERTIFY THAT THE MAJOR PROJECT ENTITLED

LOW POWER 4×4 BIT MULTIPLIER DESIGN USING DADDA ALGORITHM

IS THE BONAFIDE WORK OF

Rasamalla Anusha	16251A04G3
Goli Yaminisadhana	17255A0426
Singireddy Ramya	17255A0428
Eslavath Shivani	16251A04D5

SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIREMENT FOR THE AWARD OF DEGREE OF BACHELOR OF TECHNOLOGY IN ELECTRONICS AND COMMUNICATION ENGINEERING DURING THE YEAR 2019-2020

9/5/20

Dr.B.Venkateshulu
PROF & HOD, ECE

9/5/20

Dr.K.Ragini
GUIDE