# DEPT. OF ELECTRONICS & COMMUNICATION ENGG

## CERTIFICATE

THIS IS TO CERTIFY THAT THE MINI PROJECT ENTITLED

## DELAY ESTIMATION OF VLSI CIRCUITS THROUGH RC TIME CONSTANT USING MACHINE LEARNING

IS THE BONAFIDE WORK OF

| | |
|---|---|
| SOMAROUTHU JHANSI LAKSHMI | 17251A0485 |
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| POOJASREE KEERTHIPATI | 17251A04B0 |
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SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIREMENT FOR THE AWARD OF DEGREE OF BACHELOR OF TECHNOLOGY IN ELECTRONICS AND COMMUNICATION ENGINEERING DURING THE YEAR 2019-2020

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