DEPT. OF ELECTRONICS & COMMUNICATION ENGG

CERTIFICATE

THIS IS TO CERTIFY THAT THE MINI PROJECT ENTITLED

NOVEL HIGH SPEED VEDIC MULTIPLIER PROPOSAL INCORPORATING ADDER BASED ON QUATENERY SIGNED DIGIT NUMBER SYSTEM

IS THE BONAFIDE WORK OF

REBELLI ANUSHA	16251A04G4
JINNE DURGA	17255A0432
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SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIREMENT FOR THE AWARD OF DEGREE OF BACHELOR OF TECHNOLOGY IN ELECTRONICS AND COMMUNICATION ENGINEERING DURING THE YEAR 2018-2019

26/4/19

Dr.B.Venkateshulu

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GUIDE