

DEPT. OF ELECTRONICS & COMMUNICATION ENGG

CERTIFICATE


THIS IS TO CERTIFY THAT THE PROJECT ENTITLED

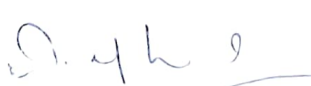
**Leakage Power Estimation in Digital VLSI Circuits Using
Support Vector Machine**

IS THE BONAFIDE WORK OF

K. VARNIKA
(18251D3807)

SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIREMENT FOR THE
AWARD OF DEGREE OF MASTER OF TECHNOLOGY IN DIGITAL ELECTRONICS
AND COMMUNICATION ENGINEERING DURING THE YEAR 2018-2019.


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