DEPT. OF ELECTRONICS & COMMUNICATION ENGG

CERTIFICATE

THIS IS TO CERTIFY THAT THE PROJECT ENTITLED

LOW-POWER AND HIGH SPEED FULL ADDER CIRCUITS USING SUB-THRESHOLD VTMOS LOGIC

IS THE BONAFIDE WORK OF

P. JUVERIA

(17251D3809)

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENT FOR THE AWARD OF DEGREE OF MASTER OF TECHNOLOGY IN DIGITAL ELECTRONICS AND COMMUNICATION ENGINEERING DURING THE YEAR 2018-2019.

4/9/19

HEAD, ECE DEPARTMENT
Dr. B. VENKATESHULU

K. Ragini

INTERNAL GUIDE
Dr. K. RAGINI
Professor, ECE Dept.

EXTERNAL EXAMINER