G.Narayanamma Institute of Technology & Science (for women)

IETE STUDENT FORUM
(2023-24)

Seminar Report on
"Current Trends in Verifying Complex Chips"

Name of the Program: - Seminar on Current Trends in Verifying Complex Chips.
Date: - 19/08/2023
Venue: - G. Narayanamma Institute of Technology & Science (for women), Hyderabad

The IETE Student Forum (ISF) unit at GNITS hosted a seminar titled "**Current Trends in Verifying Complex Chips**" from 11:30 am to 1:00 pm in Main seminar hall, GNITS by speaker Shri V. Pratyusha, Lead ASIC Verification Engineer at Moschip Semiconductors.

The seminar covered a range of topics, including VLSI (Very Large-Scale Integration), both the front end and back end aspects of chip design, and the Verilog language. This event attracted a total of 156 participants, primarily comprising 3rd and 4th-year students and 7 faculty from the ECE and ETE. During the session, Dr.K.Ragini, Head of the Department, along with faculty members and students, engaged in a fruitful discussion with the speaker.

The event's organization, theme, impact on participants' future careers, and the resource person have all received excellent ratings from the participants. This feedback highlights the event's effective planning, engaging theme, valuable career-related benefits, and the high quality of the resource person's contribution.

Fig:President, Faculty advisors, coordinators, resource persons and participants group photo.

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