DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

POWER CONVERTERS SIMULATION LAB

2023

G. Narayanamma Institute of Technology & Science

(For Women)

Shaikpet, Hyderabad – 500 104

G. Narayanamma Institute of Technology & Science (For Women)

Department of Electrical and Electronics Engineering

I Year M.Tech. II- Semester (PEED)- A.Y. 2024-25

POWER CONVERTERS SIMULATION LAB

List of Experiments

1. Simulation of Buck and Boost converter with open loop operation.
2. Simulation of Cuk and Fly Back converter with open loop operation.
3. Simulation of Z-source inverter.
4. Three Level three phase Sinusoidal PWM based H-Bridge Inverter.
5. Five Level three phase Sinusoidal PWM based H- Bridge Inverter.
6. Three Level three phase Sinusoidal PWM based Flying Capacitor Inverter.
7. Five Level three phase Sinusoidal PWM based Flying Capacitor Inverter.
8. Three Level three phase Sinusoidal PWM based Diode Clamped Inverter.
9. Five Level three phase Sinusoidal PWM based Diode Clamped Inverter.
10. Space Vector Pulse Width Modulation technique for Single phase inverter.

Additional Experiment

11. Generation of Square waveform using FPGA –Xilinx.

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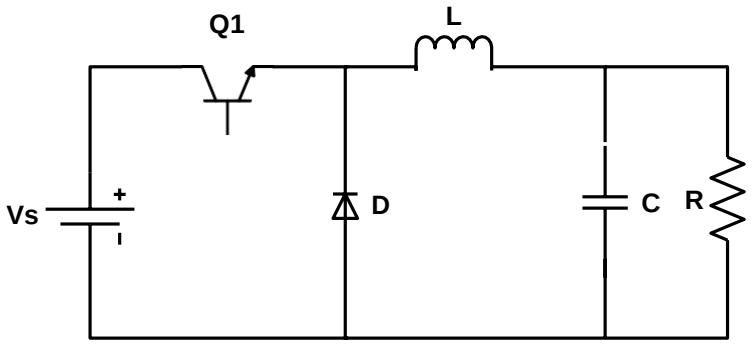
BUCK CONVERTER

Aim: To study the open loop operation of Buck Converter with R-Load using MAT LAB / SIMULINK software.

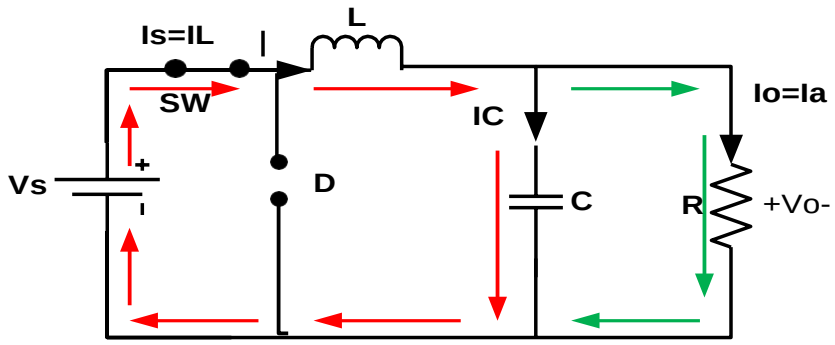
Circuit Diagram:



Theory:

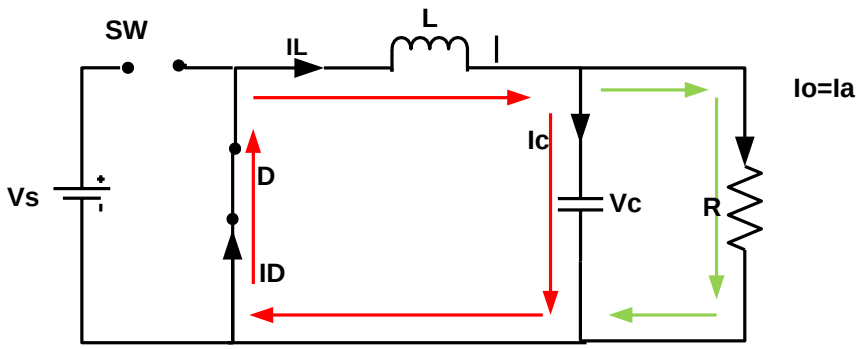
A buck converter is a dc-to-dc power converter which produces lower average output voltage that the dc input voltage . The circuit operation can be divided into two modes.

Mode-1:



When switch is ON at t=0, the input current flows through the inductor L, capacitor **C** and load **R**. The voltage across inductor, $V_L = V_s - V_o$.

Mode-2:



When switch is OFF at $t=t_1$, the diode conducts due to the energy stored in the inductor. Inductor current continues to flow through inductor L, capacitor C, diode D and load R. When the switch is opened, the voltage across the inductor is $V_L = -V_O$.

During the OFF state, the inductor current falls until switch Q1 is ON again in the next cycle. This operation is repeated for every cycle. The output voltage of the converter varies linearly with the duty cycle for a given input voltage.

$$\text{As} \quad D = \frac{T_{on}}{T}$$

Then,

$$T_{on} = DT$$

$$T_{off} = (1-D)T$$

$$\text{Inductor, } L = \frac{V_s D(1-D)}{f\Delta I}$$

$$\text{Capacitor, } C = \frac{V_s D(1-D)}{8L\Delta V_c f^2}$$

As the buck converter requires only one transistor, it is simple and has high efficiency approx. greater than 90%.

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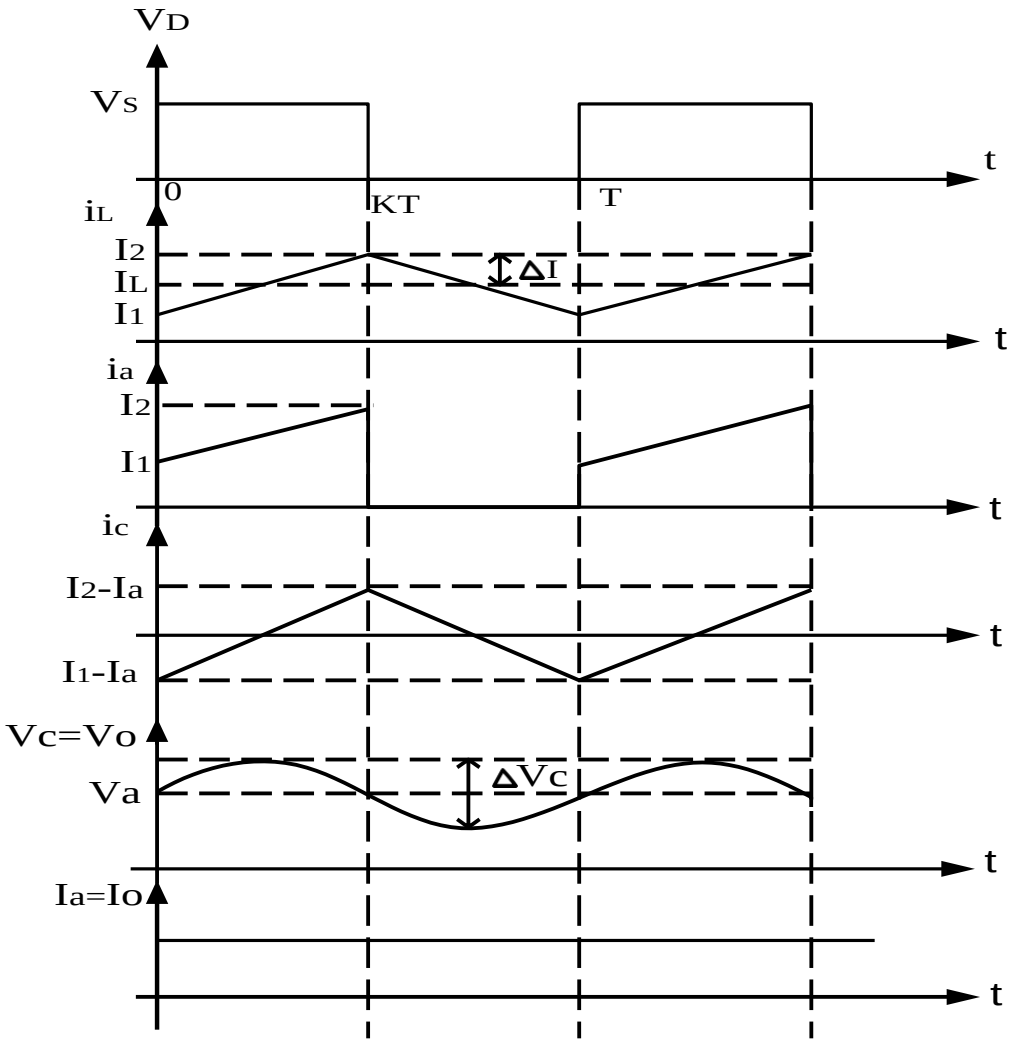
Theoretical Waveforms:



Design Specifications:

Assume: $V_s = 50V$; $D = 0.5$; $P = 50W$; and Frequency, $f = 25KHz$

$\rightarrow Vo = DV_s \Rightarrow V_o = 0.5 \times 50$

$\therefore V_o = 25V$

$\rightarrow P_o = I^2R \Rightarrow P_o = \frac{V_o^2}{R}$ $\left[\because I = \frac{V}{R} \right] \Rightarrow 50 = \frac{25^2}{R}$

$\therefore R = 12.5\Omega$

$$\rightarrow I_o = \frac{V_o}{R} \Rightarrow I_o = \frac{25}{12.5}$$

$$\therefore I_o = 2A$$

Assume that $\Delta I = 0.1A;\ \Delta V_c = 0.1V$

$$\rightarrow L = \frac{V_s D(1-D)}{f\Delta \mathrm{I}} \Rightarrow L = \frac{50 \times 0.5(1-0.5)}{25 \times 1000 \times 0.1}$$

$$\therefore L = 5mH$$

$$\rightarrow C = \frac{V_s D(1-D)}{8L\Delta V_c f^2} \Rightarrow C = \frac{50 \times 0.5 \times (1-0.5)}{8 \times 5 \times 10^{-3} \times 0.1 \times (25 \times 10^3)^2}$$

$$\therefore C = 5\mu F$$

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. The inductor and capacitor values are chosen as per the theoretical calculations.
3. The circuit is simulated for variable duty cycle and for various load values.
4. The current through inductor, voltage across inductor ,current through capacitor , voltage across capacitor and output voltage ,current waveforms are traced for all conditions.

Simulation Waveforms:

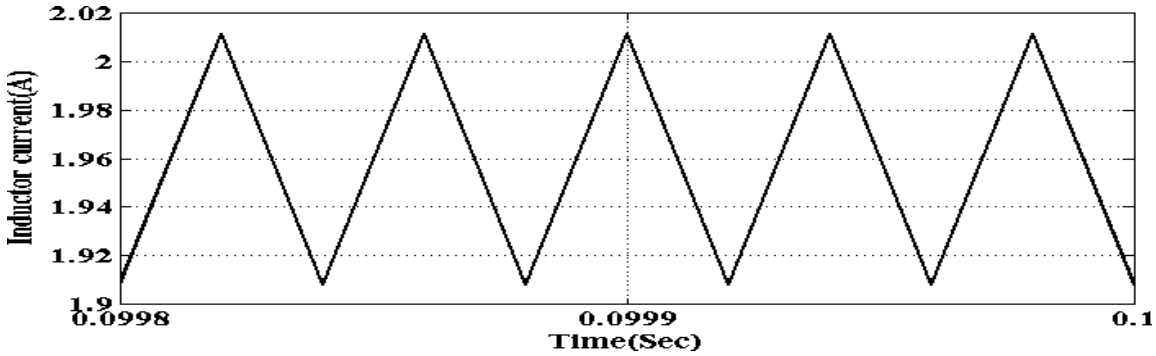


Fig1. Current through the inductor.

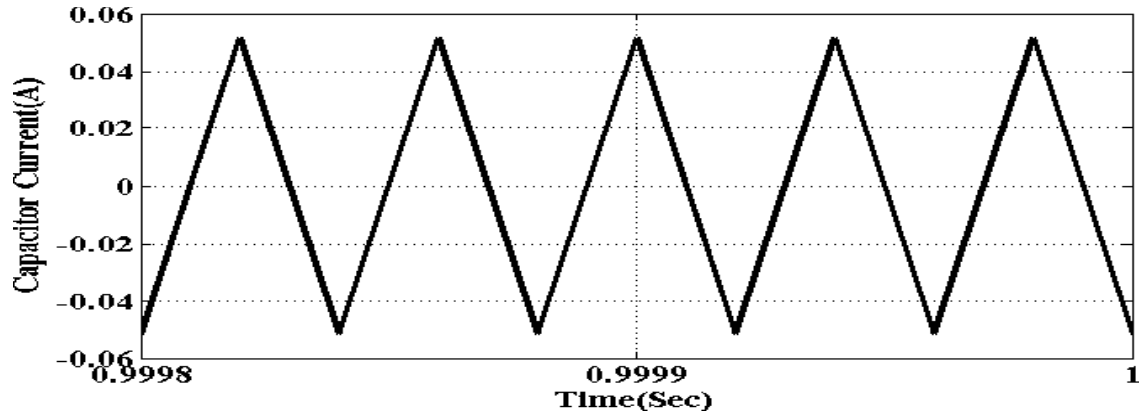


Fig.2. Current through the capacitor.

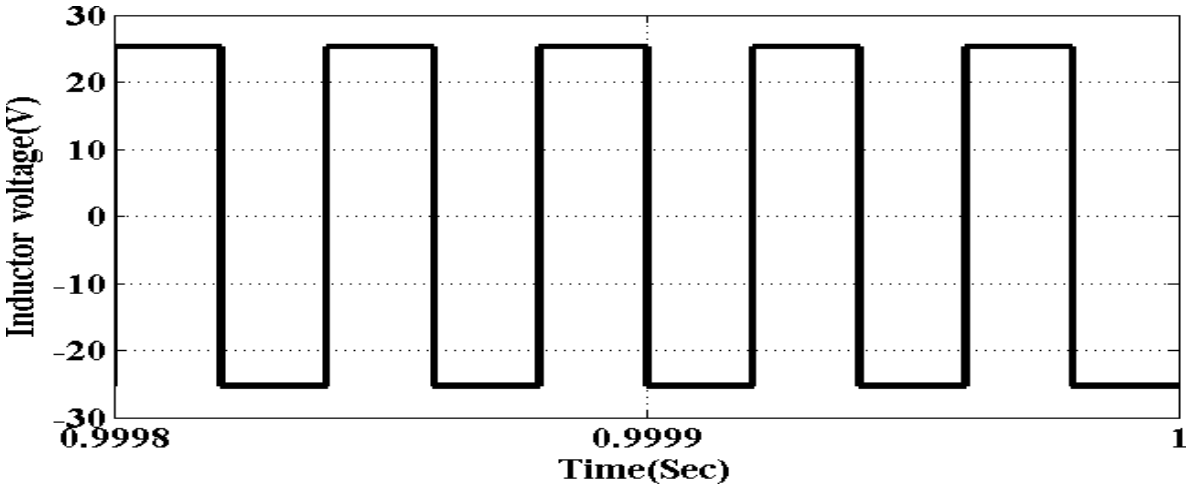


Fig.3 Voltage across inductor

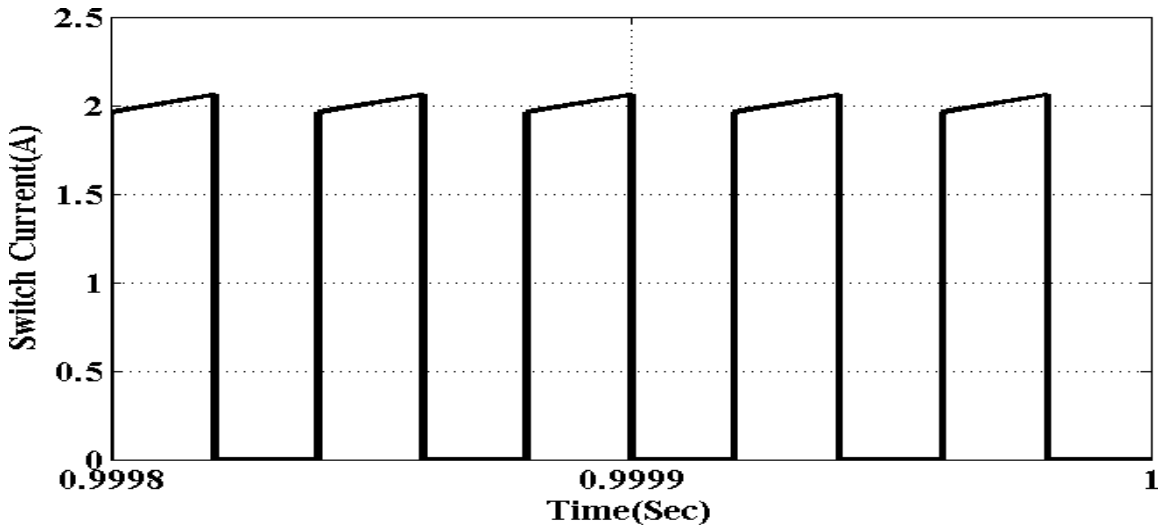


Fig.4. Current through the switch

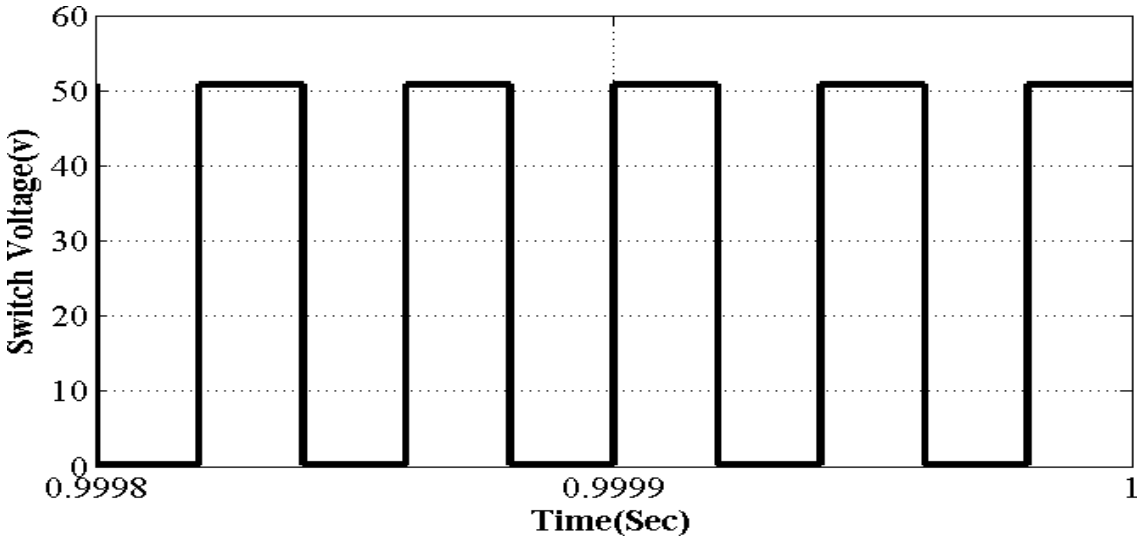


Fig.5 Voltage across Switch.

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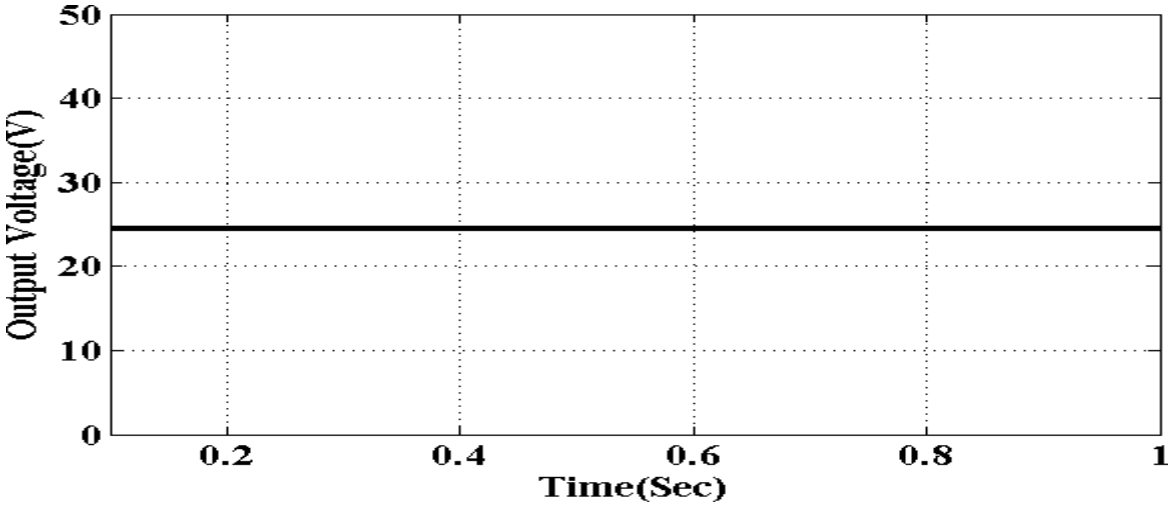

Fig. Output Voltage across R load

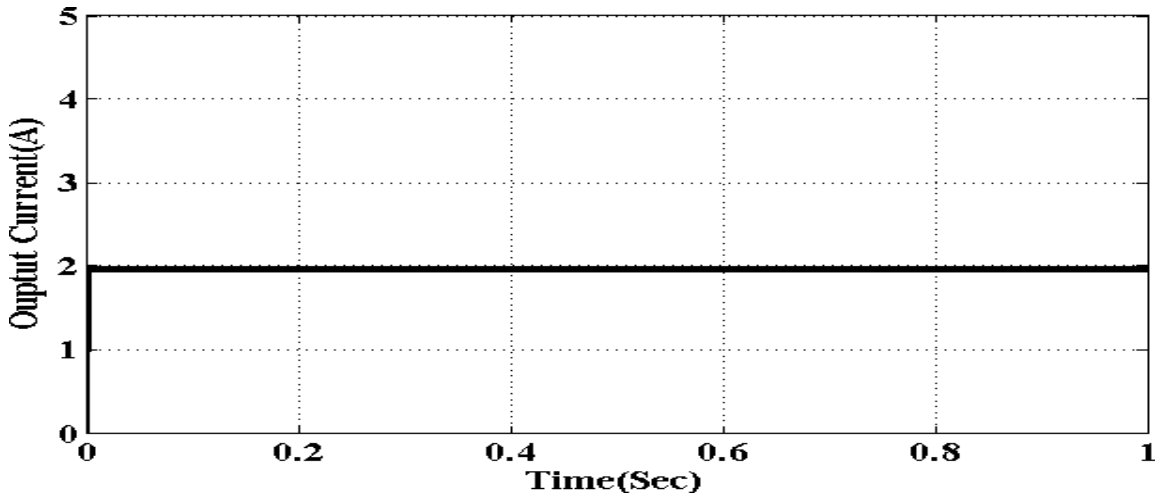

Fig. Output Current through Resistor.

Result : The buck converter is simulated using MATLAB/SIMULINK and its operation is studied using various waveforms.

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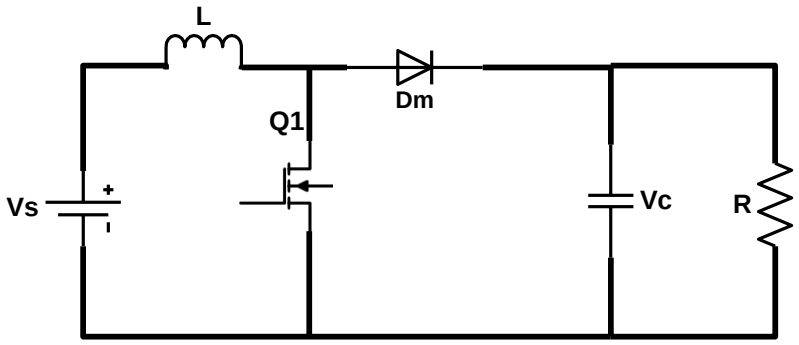
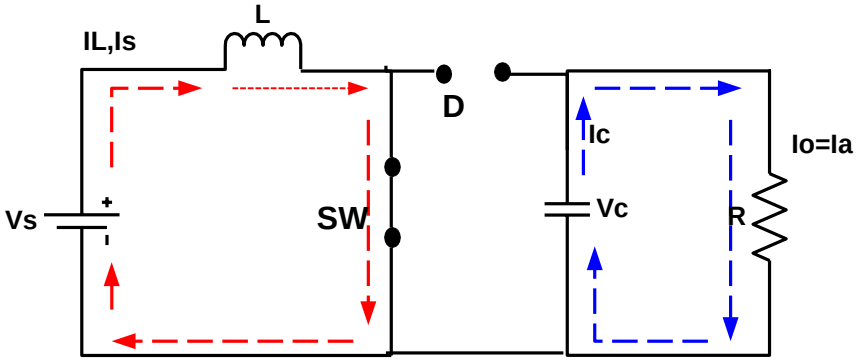
BOOST CONVERTER

Aim: To study the open loop operation of Boost Converter with R-Load using MAT LAB / SIMULINK software.

Circuit Diagram:

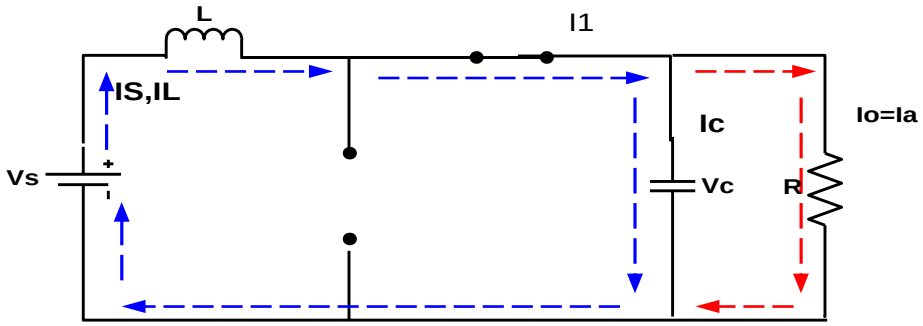


Mode-1



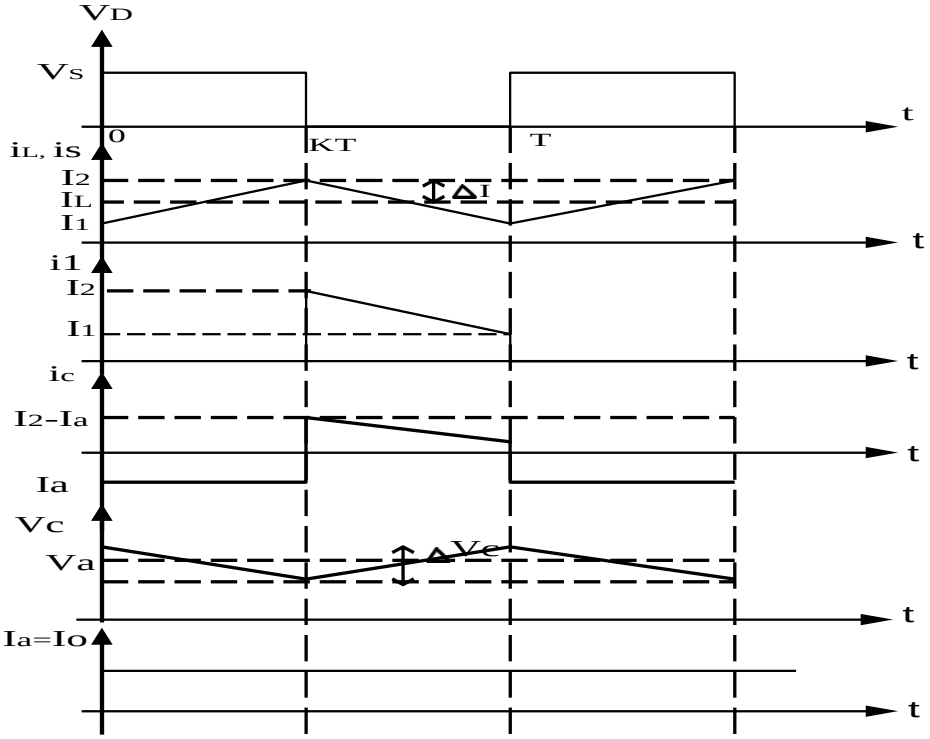
When the switch is ON at t=0, the input current rises and flows through inductor L and switch SW.

Mode-2



Mode – 2 begins when transistor is switched OFF at t = t1, the current that was flowing through the transistor would now flow through L, C, load, and diode. When the switch is OFF the energy stored in the inductor is released to the load.

Theoretical waveforms:



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Formulae related to Boost Converter:

$V_o = \frac{V_s}{1-D}$, $I_o = I_s(1-D)$, $L = \frac{V_s D}{f\Delta \mathrm{I}}$ and $C = \frac{I_o D}{f\Delta V_c}$

Design Specifications:

Assume $V_s = 50V$; $D = 0.5$; $P = 100W$: $f = 25KHz$

$\rightarrow V_o = \frac{V_s}{1-D} \Rightarrow \frac{50}{1-0..5} = 100V$

$\rightarrow P_o = \frac{V_o^2}{R} \Rightarrow \frac{100^2}{100} = 100\Omega$

$\rightarrow I_o = \frac{V_o}{R} \Rightarrow \frac{100}{100} = 1A$

$\rightarrow L = \frac{V_s D}{f\Delta \mathrm{I}} = \frac{50 \times 0.5}{25 \times 10^3 \times 0.1} = 0.01H = 10mH$ $\left(\because Assume\ \Delta \mathrm{I} = 0.1\right)$

$\rightarrow C = \frac{I_o D}{f\Delta V_c} = \frac{1 \times 0.5}{25 \times 10^3 \times 0.1} \Rightarrow 0.0002F = 200\mu F$ $\left(\because Assume\ \Delta V_c = 0.1\right)$

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. The inductor and capacitor values are chosen as per the theoretical calculations.
3. The circuit is simulated for variable duty cycle and for various load values.
4. The current through inductor, voltage across inductor ,current through capacitor , voltage across capacitor and output voltage ,current waveforms are traced for all conditions.

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Simulation Results:

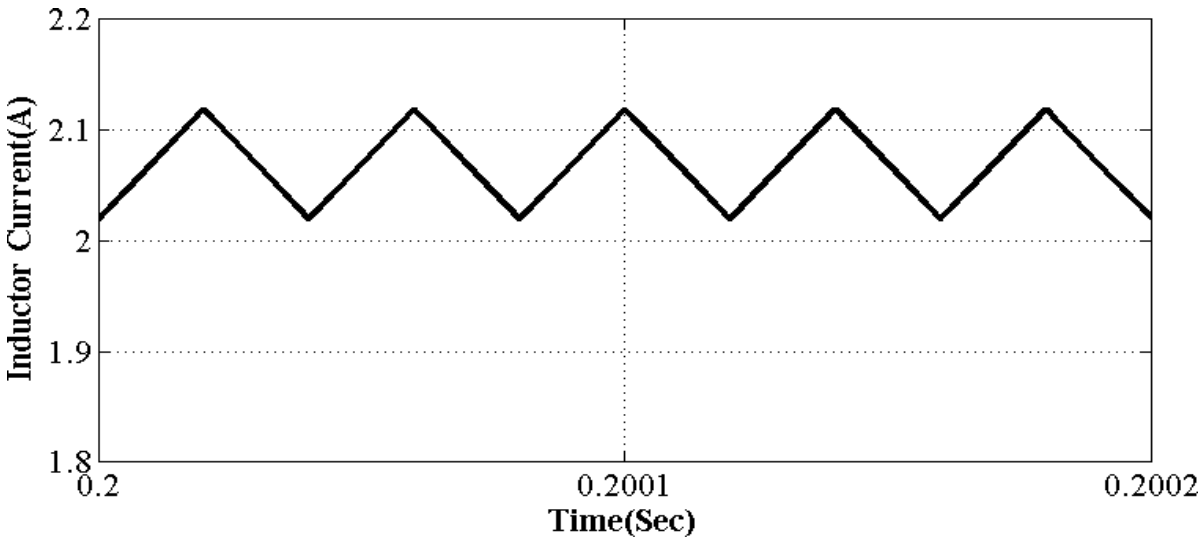

Fig.1. Current through Inductor current (A)

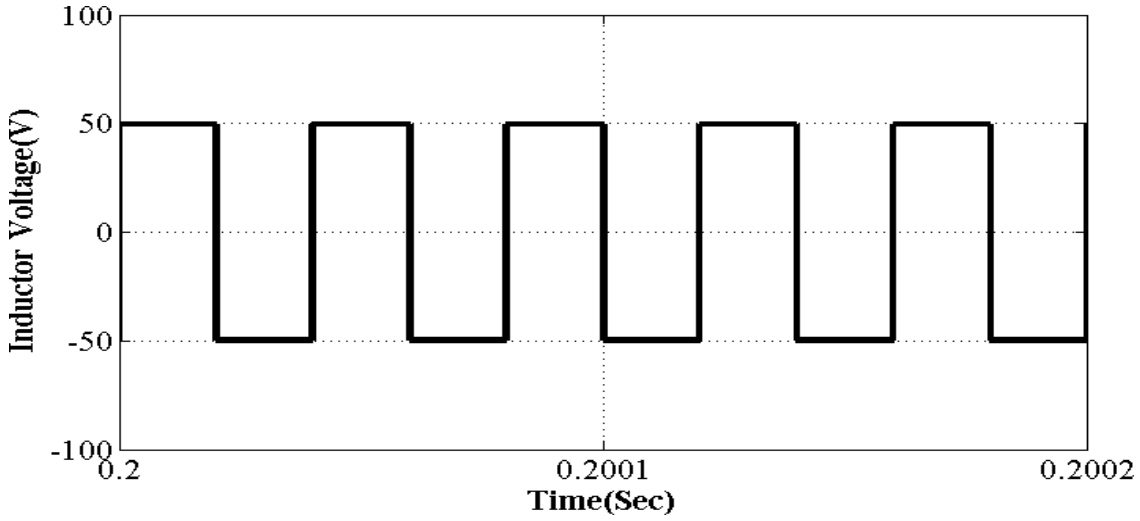

Fig.2. Voltage Across Inductor (V)

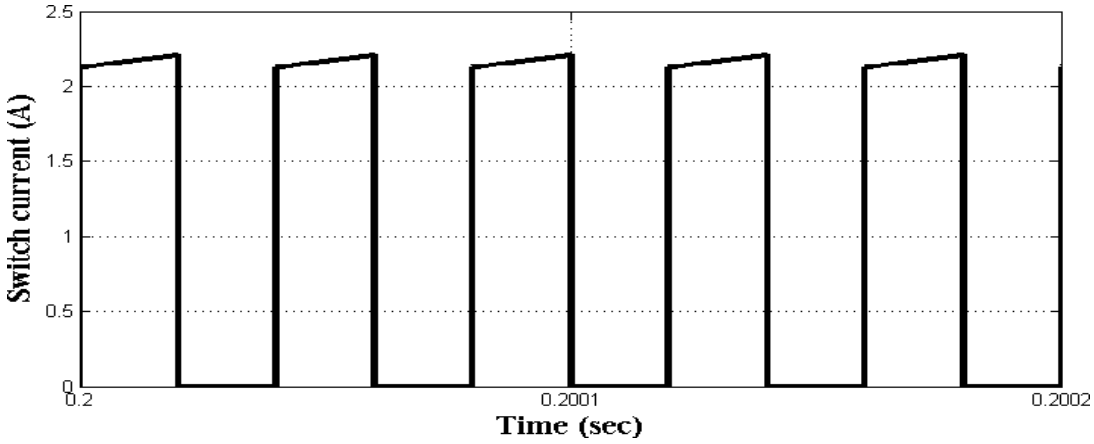

Fig.3. Current through the Switch (A)

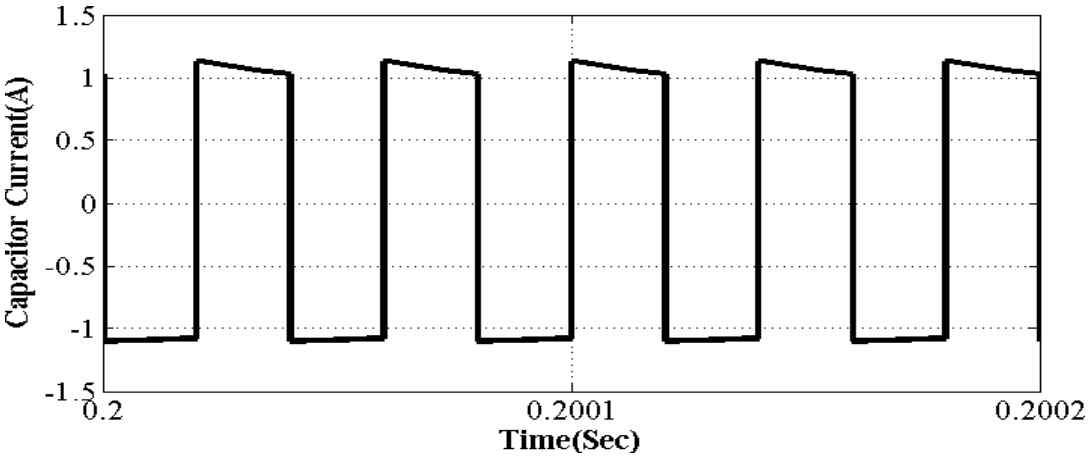

Fig .4. Current Through the Capacitor. (A)

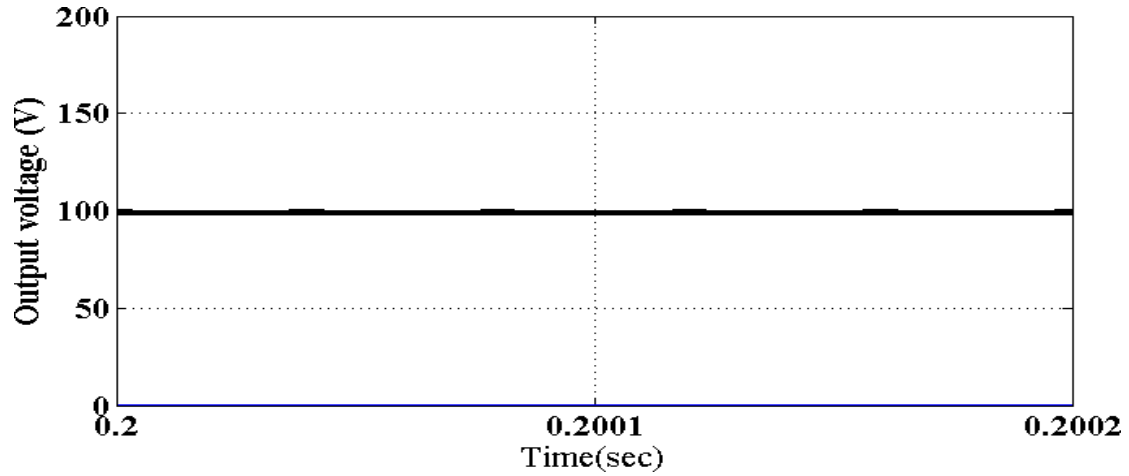

Fig .5. Output voltage across the load (V)

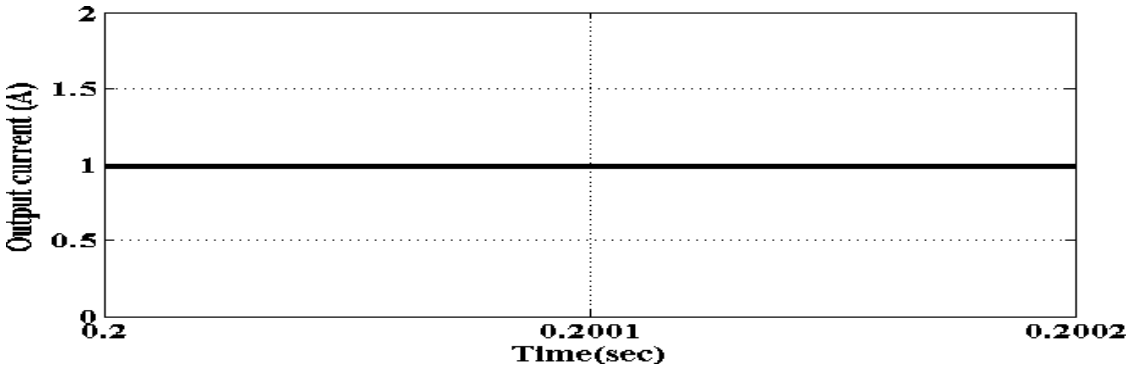

Fig.6.Output current through the load.(A)

Result : The boost converter is simulated using MATLAB/SIMULINK and its operation is studied using various waveforms.

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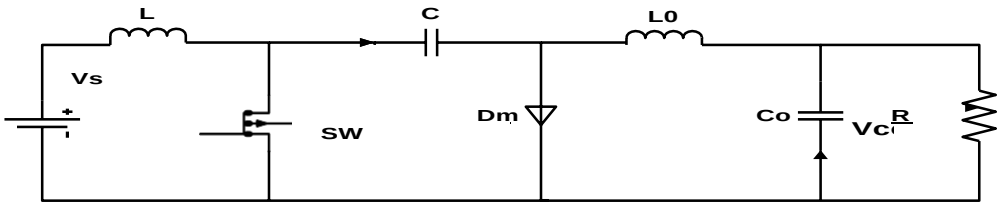
CUK CONVERTER

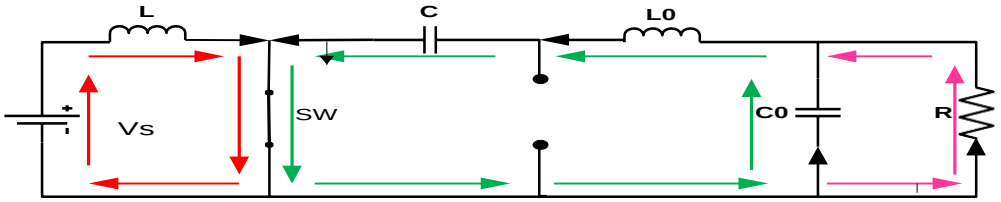
Aim: To study the open loop operation of Cuk Converter with R-Load using MAT LAB / SIMULINK software.

Circuit diagram:



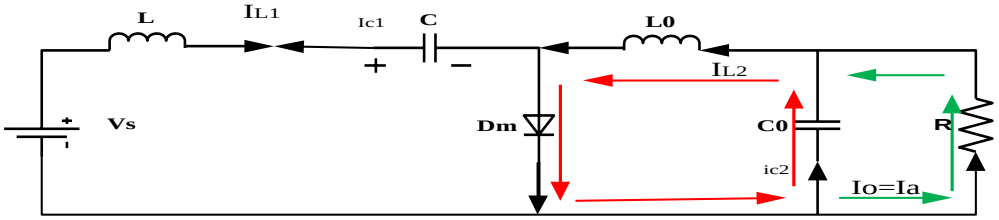
Theory: A Cuk converter is a dc-to-dc power converter which produces output voltage either greater than or less than the dc input voltage . The circuit operation can be divided into two modes.

Mode 1:



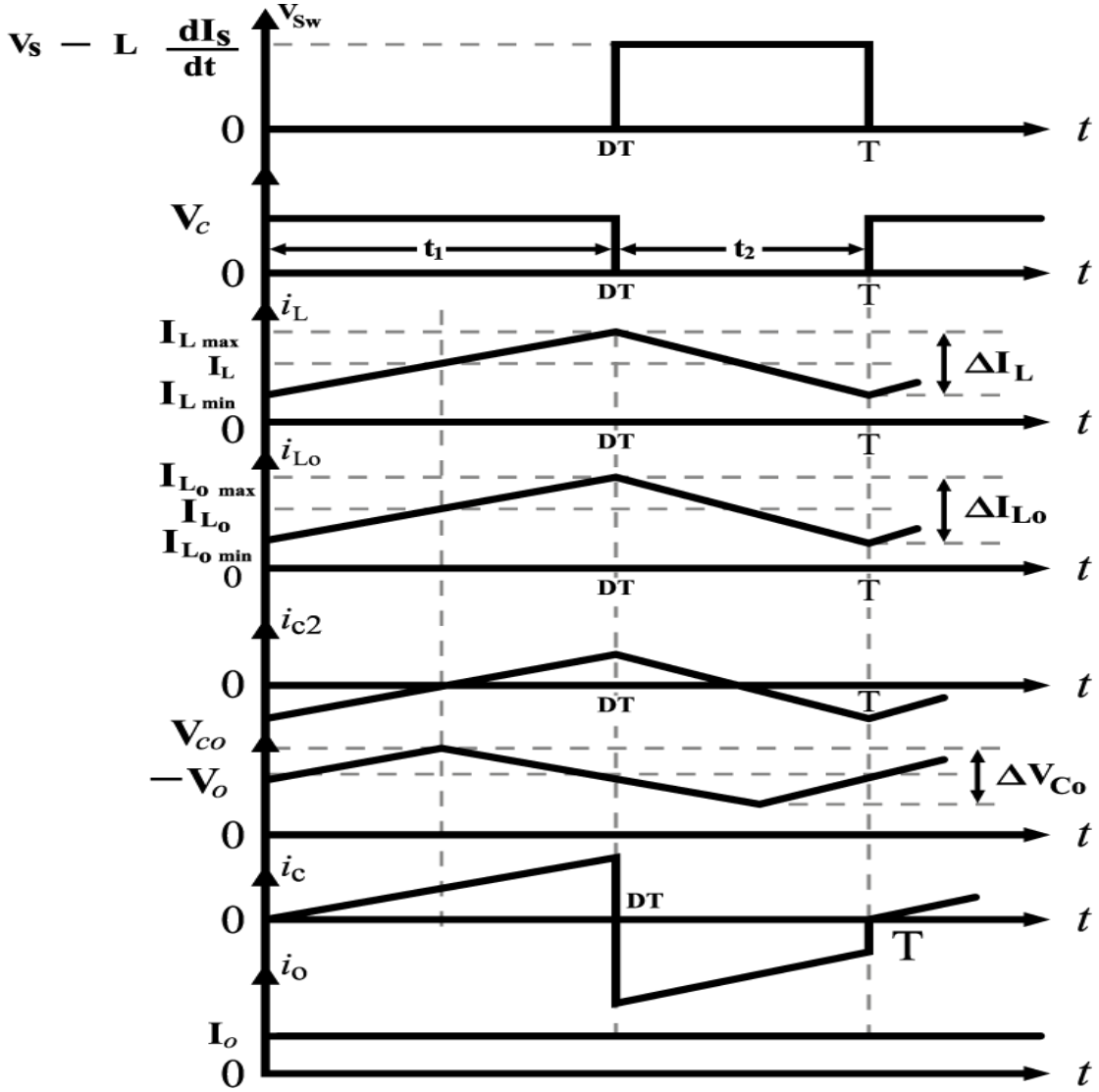
When the switch is turned ON at t=0, the current through inductor L rises. At the same time the voltage across capacitor C reverse bias diode D and is turned OFF. The capacitor C discharges its energy to the circuit formed by C, Co and Lo.

Mode2:



when the switch is turned OFF at t=t, the capacitor C is charged from the input supply and the energy stored in the inductor Lo is transferred to the load. The diode D and switch SW provides a synchronous switching action. The capacitor C is the medium for transferring energy from the source to the load.

Theoretical Waveforms:



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Formulae related to Cuk converter:

$$V_o = \frac{-V_s D}{1-D} \quad I_s = \frac{I_a D}{1-D}$$

$$\Delta I_1 = \frac{V_s D}{fL_1}, \quad \Delta I_2 = \frac{V_s D}{fL_2}$$

$$\Delta V_{c1} = \frac{I_s(1-D)}{fC_1}, \Delta V_{c2} = \frac{V_s D}{8C_2 L_2 f^2}$$

Design Specifications: Assume: $V_s = 100V$; $f = 50KHz$; $D = 0.5$

$$\rightarrow V_o = \frac{-V_s D}{1-D} = \frac{-100 \times 0.5}{1-0.5} = 100V$$

$$\rightarrow I_s = \frac{I_a D}{1-D} = \frac{0.5 \times 10}{1-0.5} = 10A$$

$$\rightarrow \Delta I_1 = \frac{V_s D}{fL} = \frac{100 \times 0.5}{50000 \times 1 \times 10^{-3}} = 1A$$

$$\rightarrow \Delta I_2 = \frac{V_s D}{fL_0} = \frac{0.5 \times 100}{50000 \times 1 \times 10^{-3}} = 1A$$

$$\rightarrow \Delta V_{c1} = \frac{I_s(1-D)}{fC} = \frac{10(1-0.5)}{50000 \times 47 \times 10^{-6}} = 2.12V$$

$$\rightarrow \Delta V_{c2} = \frac{V_s D}{8C_0 L_0 f^2} = \frac{0.5 \times 100}{8 \times 47 \times 10^{-6} \times 1 \times 10^{-3} \times 50000^2} = 0.05V$$

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. The inductor and capacitor values are chosen as per the theoretical calculations.
3. The circuit is simulated for variable duty cycle and for various load values.
4. The current through inductor, voltage across inductor ,current through capacitor , voltage across capacitor and output voltage ,current waveforms are traced for all conditions.

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Simulation waveforms:

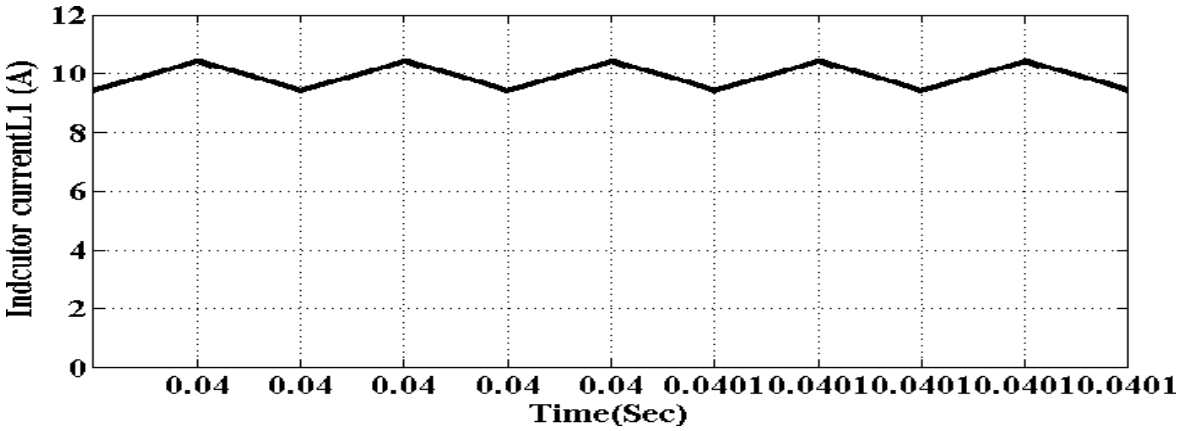

Fig.1. Current through inductor L

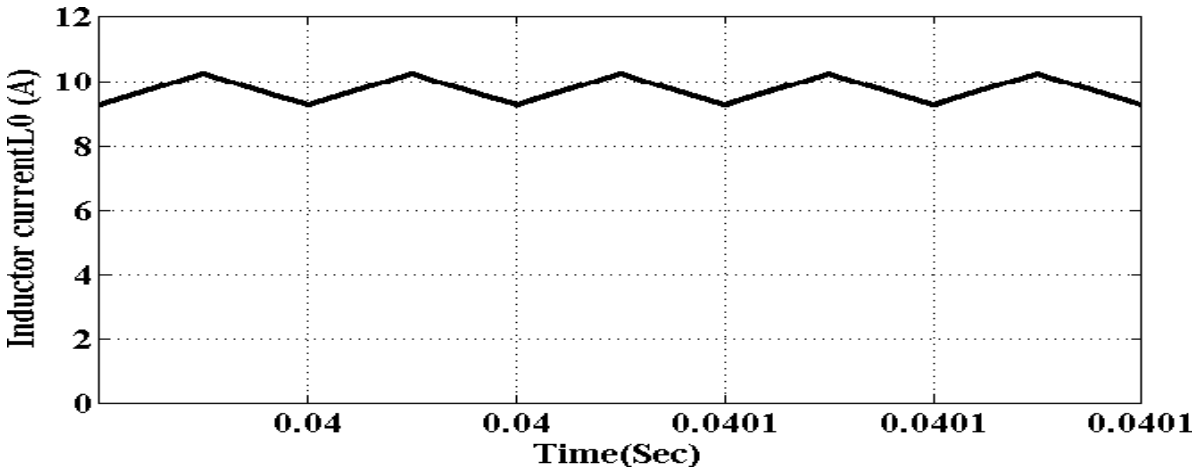

Fig.2. Current through inductor L0

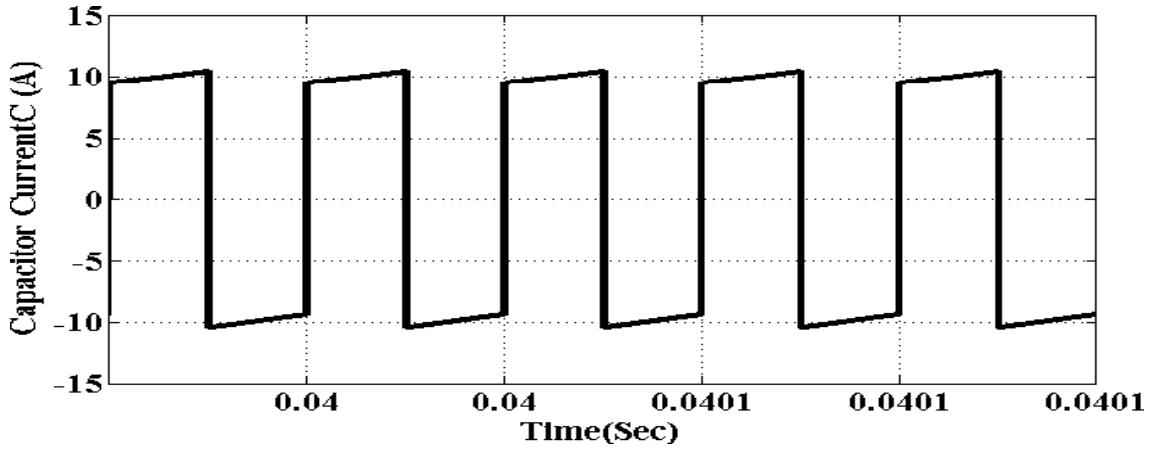

Fig.3.Current through capacitor current C(A)

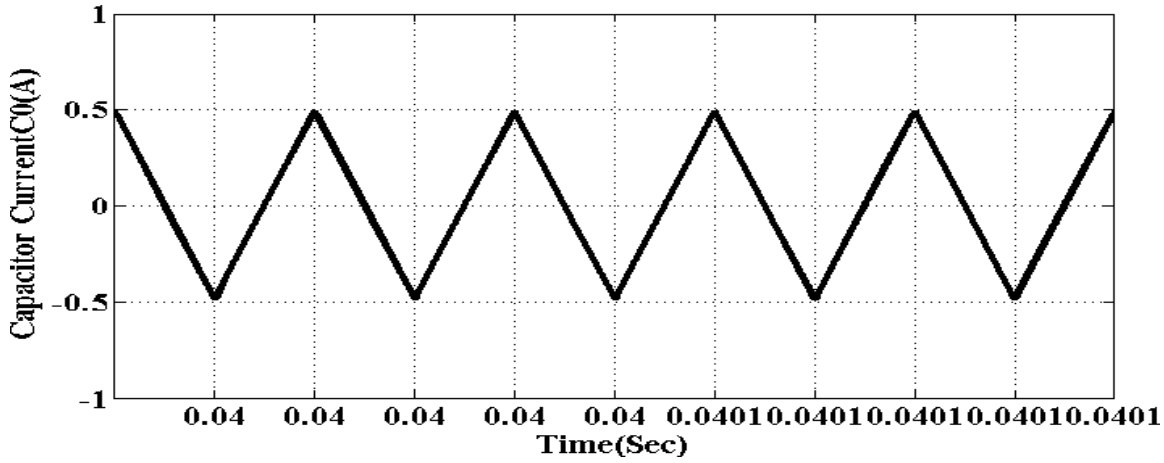

Fig.4.Current through capacitor current C0(A)

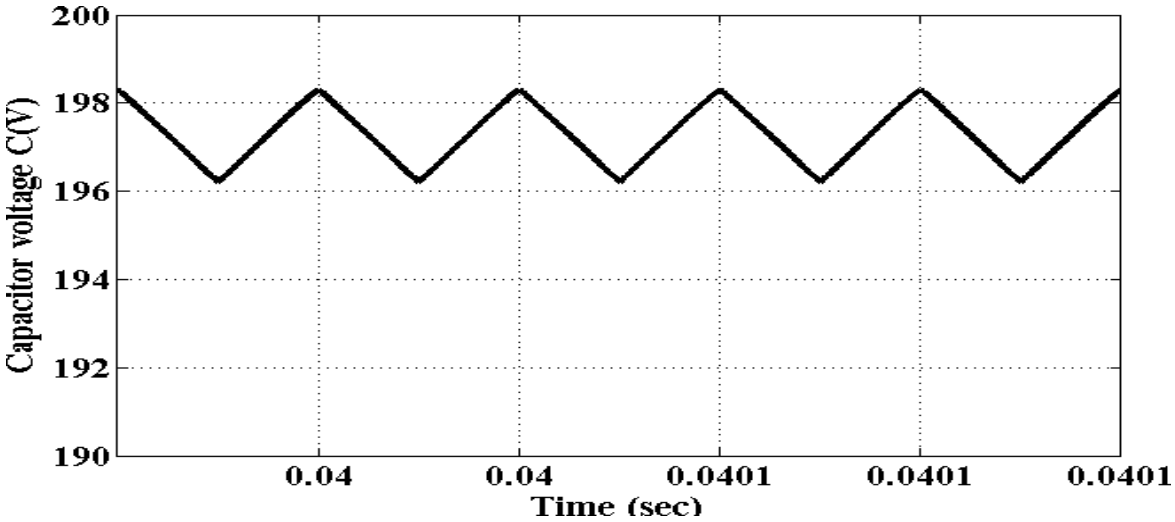

Fig.5.Capacitor voltage C(V)

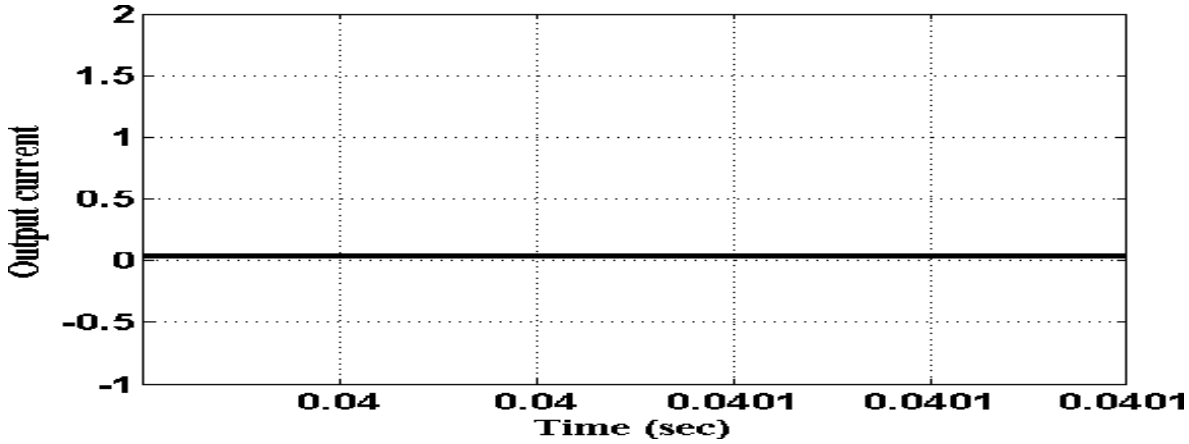

Fig.6.Output current through R load

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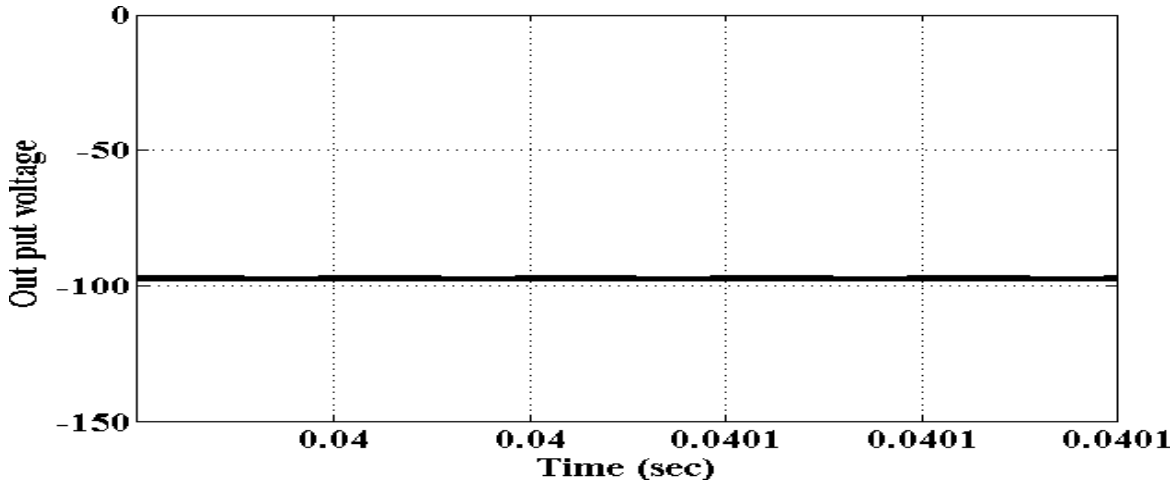

Fig.7. Output voltage across R load

Result : The cuk converter is simulated using MATLAB/SIMULINK and its operation is studied using various waveforms.

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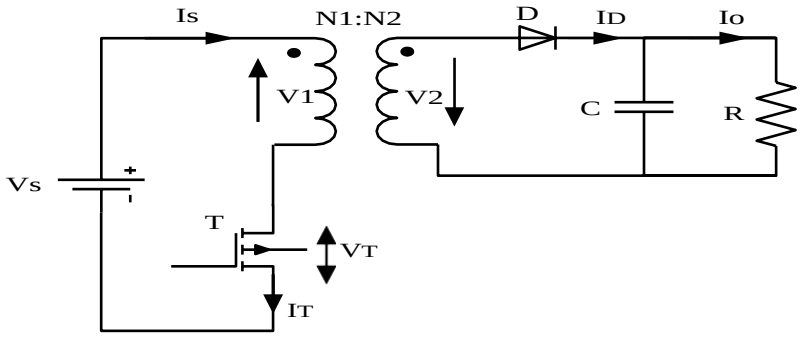
FLY- BACK CONVERTER

Aim: To study the open loop operation of Fly-Back Converter with R-Load using MAT LAB / SIMULINK software.

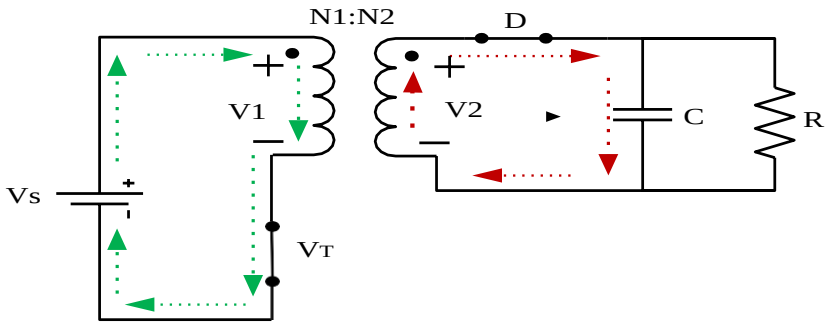
Circuit Diagram:



Theory:

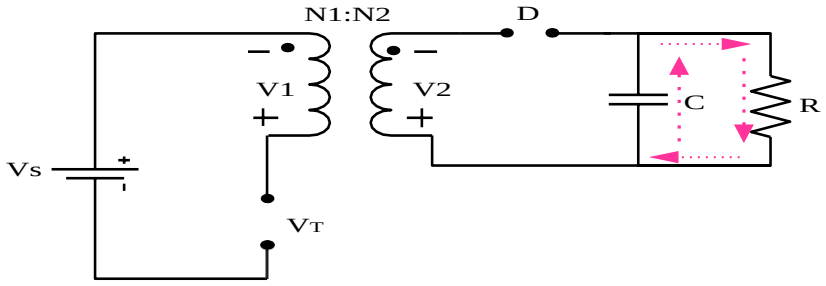
Fly-back converter is derived from the buck –boost converter .By placing a second winding on the inductor, it is possible to achieve electrical isolation. The circuit operation can be divided into two modes.

Mode-1:



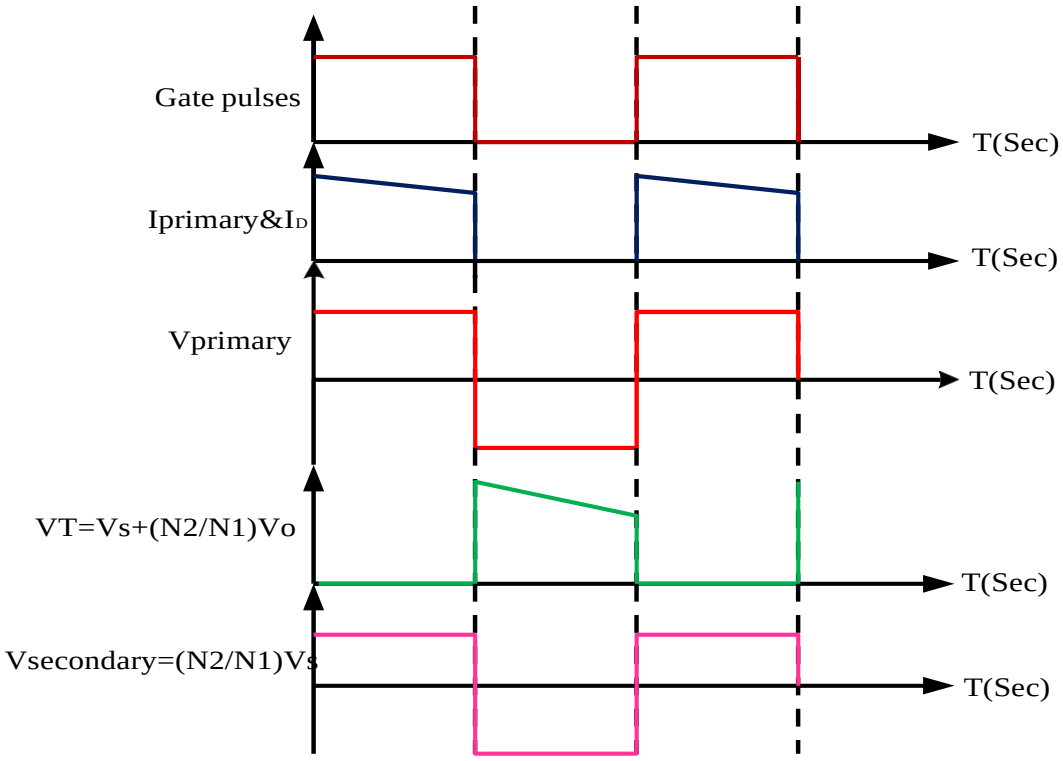
When Switch is ON, input current flows through the transformer primary winding V_1, switch V_T and to $-V_S$. Due to transformer action, voltage is induced in the secondary winding and current start flowing through diode D and capacitor C resulting the capacitor to charge.

Mode-2:



When Switch is 'OFF' the transformer secondary winding V_2 is de-energized and so the diode gets turned OFF and as a result, the capacitor start discharging through the load.

Theoretical Waveforms:



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Design Specifications:

Assume V_S= 24 =V_1, f = 100KHz, R=48Ω, D = 0.5

$$V^O = \left(\frac{V_S D}{1-D}\right)\left(\frac{N_S}{N_P}\right)$$

Turns Ratio = $\frac{N_S}{N_P} = 2$

$$V_O = \left(\frac{24 \times 0.5}{1-0.5}\right)(2)$$

$V_O = 48V$

$I_O = \frac{V_O}{R} = \frac{48}{48} = 1A$ = $I_{Secondary}$

$P_O = V_O I_O = 48 \times 1 = 48W$

Magnetizing Inductance of Transformer

For discontinuous mode: $L_P = \frac{V_S D}{f I_P}$

$$L_P = \frac{24 \times 0.05}{100 \times 10^3 \times 4.13}$$

L_P = 29 µH

For Continuous mode of operation, the inductance value must be large and hence it is chosen as

L_P = 290 µF

$\frac{V_S}{V_P} = \frac{I_P}{I_S}$, $\frac{48}{24} = \frac{I_P}{1}$

$I_P = 2A$.

$V_{SW} = V_{SOURCE} + \frac{Np}{Ns} x\ V_0$

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Procedure:

1. Rig up the circuit as per the circuit diagram.
2. The inductor and capacitor values are chosen as per the theoretical calculations.
3. The circuit is simulated for variable duty cycle and for various load values.
4. The current through inductor, voltage across inductor ,current through capacitor , voltage across capacitor and output voltage ,current waveforms are traced for all conditions.

Simulated Output Waveforms:

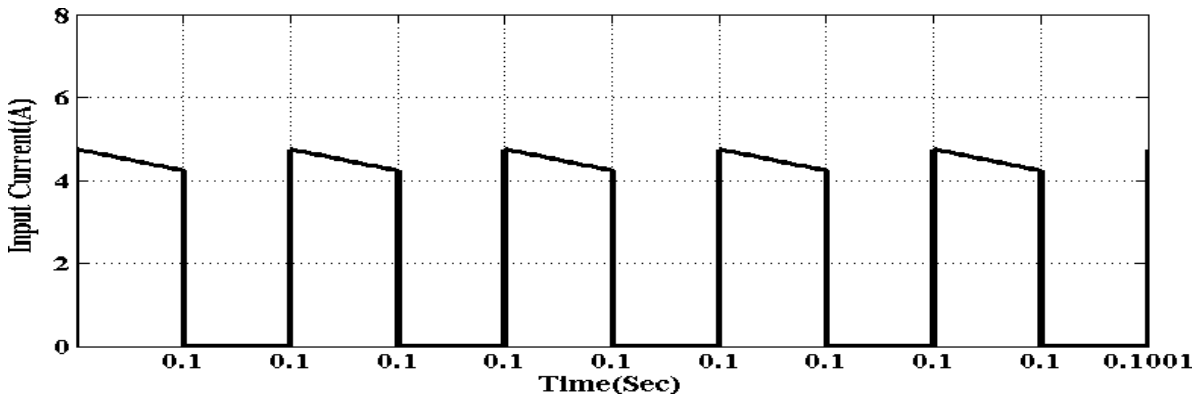

Fig.1 Input Current(A) or Primary Current(A)

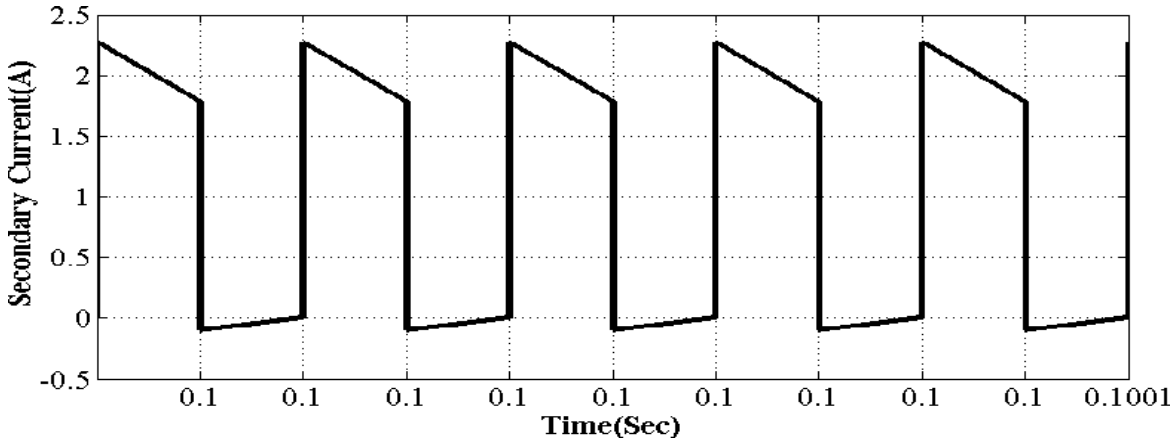

Fig.2. Secondary Current(A)

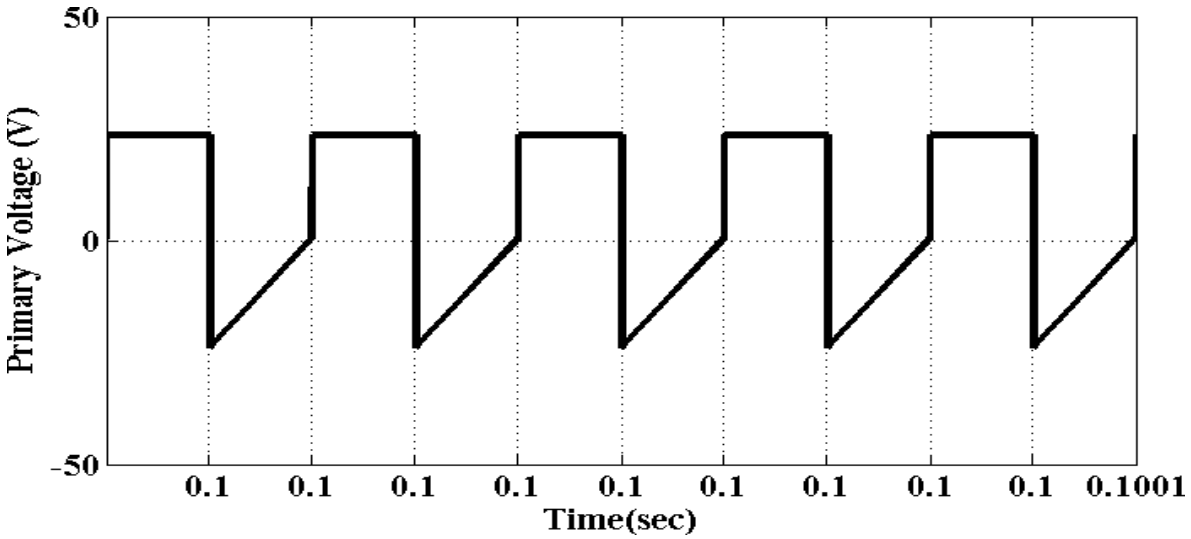

Fig.3.Primary Voltage (V)

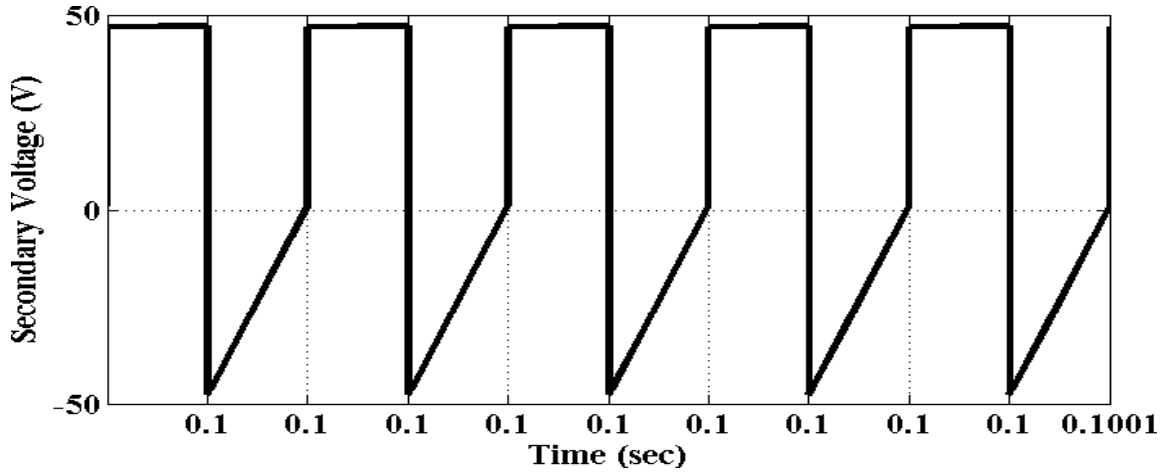

Fig.4. Secondary Voltage

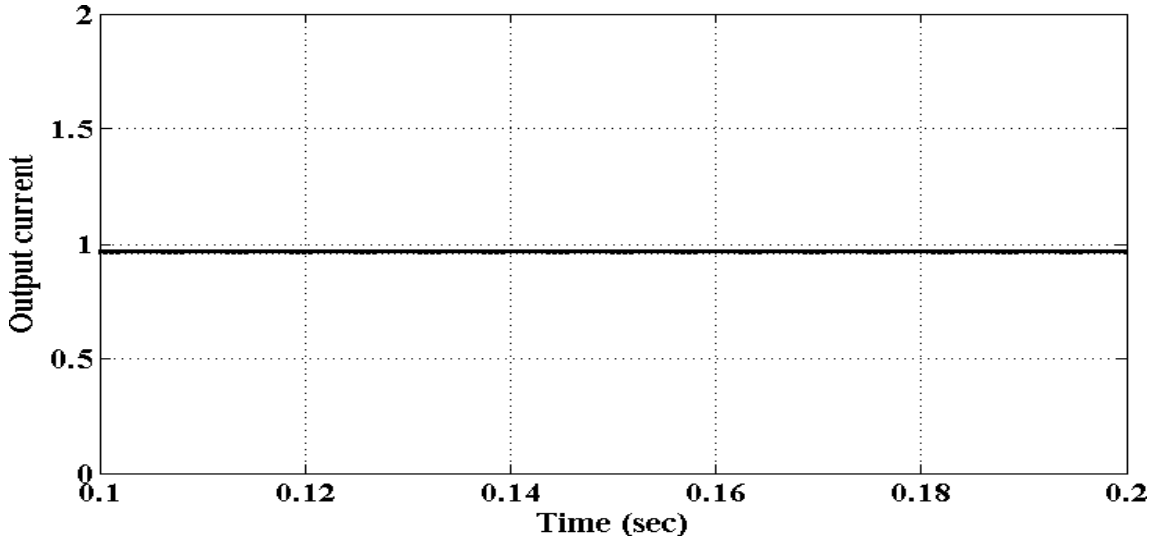

Fig.5. Output Current

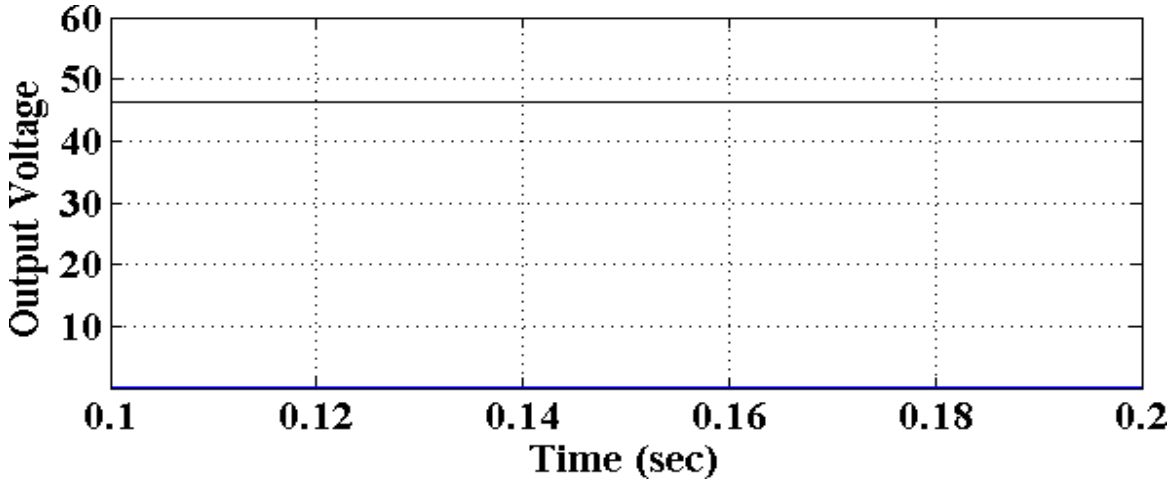

Fig.6.Output voltage(V)

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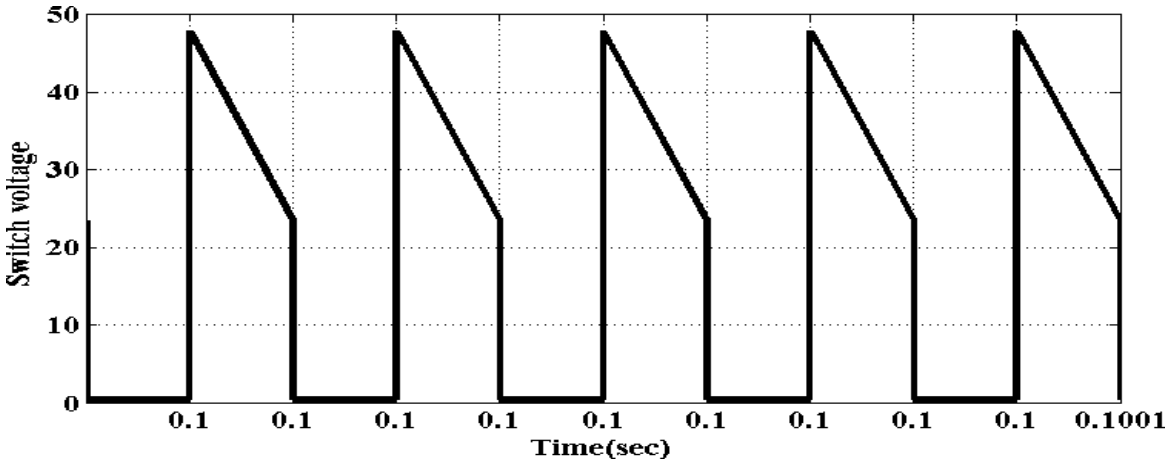

Fig.7. Switch voltage

Result : The Fly-Back converter is simulated using MATLAB/SIMULINK and its operation is studied using various waveforms.

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Z-SOURCE INVERTER

Aim: To study the Z-Source Inverter with R-Load using MATLAB / SIMULINK software.

Circuit Diagram:

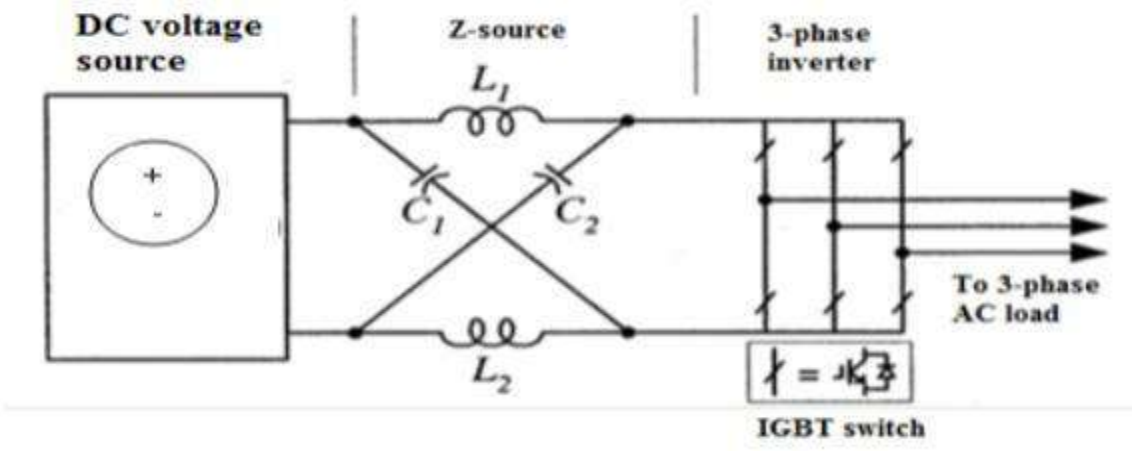


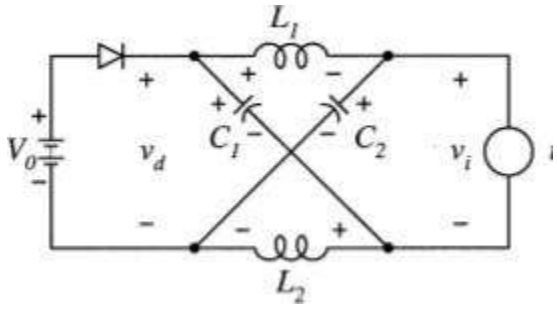
Fig. 1 Z – Source inverter

Theory:

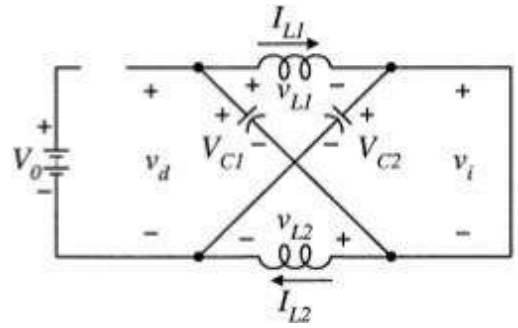
The Z-source inverter is a buck–boost inverter that has a wide range of obtainable voltage. The traditional V- and I-source inverters cannot provide such feature. To describe the operating principle and control of the Z-source inverter, the three-phase Z-source inverter bridge has nine permissible switching states (vectors) unlike the traditional three-phase V-source inverter that has eight. The traditional three-phase V-source inverter has six active vectors when the dc voltage is impressed across the load and two zero vectors when the load terminals are shorted through either the lower or upper three devices, respectively. However, the three-phase Z-source inverter bridge has one extra zero state(or vector) when the load terminals are shorted through both the upper and lower devices of any one phase leg (i.e., both devices are gated on), any two phase legs, or all three phase legs. This shoot-through zero state (or vector) is forbidden in the traditional V-source inverter, because it would cause a shoot-through.

We call this third zero state (vector) the shoot-through zero state (or vector), which can be generated by seven different ways: shoot-through via any one phase leg, combinations of any two phase legs, and all three phase legs. The Z-source network makes the shoot-through zero state possible. This shoot-through zero state provides the unique buck-boost feature to the inverter.

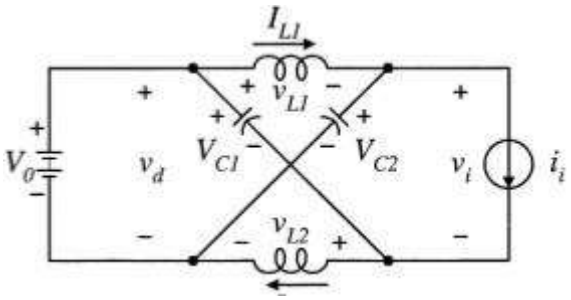
Mode-1: Equivalent circuit of the Z-source inverter viewed from the dc link.



Mode-2: Equivalent circuit of the Z-source inverter viewed from the dc link when the inverter bridge is in the shoot-through zero state.



Mode-3: Equivalent circuit of the Z-source inverter viewed from the dc link when the inverter bridge is in the shoot-through zero state.



Analysis of Impedance Network:

For simplicity, assuming that the inductors L1 and L2 and capacitorsC1 and C2 have the same inductance and capacitance respectively, the Z-source network become symmetrical.

From the symmetry and the equivalent circuits, we have

$$V_{C1}=V_{C2}= V_C \text{----------(1)}$$

$$V_{L1}=V_{L2}=V_L \text{----------(2)}$$

Given that the inverter bridge is in the shoot-through zero state for an interval ofT_0, during aswitching cycle, T and from the equivalent circuit, one has

$$V_L=V_C \ ;V_d=2V_c; \ V_i=0 \ ;$$

Now consider that the inverter bridge is in one of the eight non shoot-through states for aninterval of T1, during the switching cycle. From the equivalent circuit, one has

$$V_L=V_0-V_d \text{----------(3)}$$

$$V_d=V_0;$$

$$V_i=Vc-V_L=V_C-(V_0-V_C)V_i$$

$$=2V_c-V_0 \text{----------(4)}$$

Where V_O is the DC source voltage and $T=T_0+T_1$ ---------- (5)

The average voltage of the inductor over one switching period should be zero in steady state,

thus,

$$V_L=[T_0V_C+T_1(V_0-V_C)]/T=0$$

$$V_L=(T_0V_C+V_0T_1-V_CT_1)/T=0$$

$$V_L=[(T_0-T_1)*V_C/T]+[(T_1V_0)/T]$$

$$(V_C/V_0)=(T_1/T_1-T) \text{ ----------(6)}$$

Similarly, the average DC link voltage across the inverter bridge can be found as follows.

From equation 4:

$$V_i=[T_0 * 0+T_1(2V_c-V_0)] /T$$

$$2V_C=V_0 \text{ ---------- (7)}$$

From equation 6:

$$V_C=V_0*T_1/(T_1-T_0)$$

The peak DC-link voltage across the inverter bridge is

$$V_i=V_c-V_L=2V_C-V_0$$

$$=T/(T1-T0) *V_0=B*V_0 \text{ ----------(8)}$$

Where $B=T/(T_1-T_0) \geq 1$ ---------- (9)

B is a boost factor

The output peak phase voltage from the inverter

$$V_{out}=B*V_0 /2\ldots\ldots\ldots (10)$$

In this source

$V_{out}=MB*V_0 /2$Where M is the modulation index

The output voltage can be stepped up and down by choosing an appropriate buck - boost factor B*

B*= B.M (it varies from 0 to α) (11)

The capacitor voltage can be expressed as

$$V_{C1}=V_{C2}= V_C =(1-T_0/T)*V_C /(1-2T_0/T)$$

The boost factor B is determined by the modulation index M. The boost factor B can becontrolled by duty cycle of the shoot-through zero state over the non-shoot through states of the PWMinverter. The shoot-through zero state does not affect PWM control of the inverter. Because, itequivalently produces the same zero voltage to the load terminal, the available shoot-through period islimited by the modulation index.

Pulse Width Modulation Schemes:

The basic idea to control the ZSI is to turn traditional zero state into shoot-through zero state, while keeping the active vectors unchanged, thus we can maintain the sinusoidal output and at the same time achieve voltage boost from the shoot-through of the dc link. Actually, this control strategy inserts shoot through in all the PWM traditional zero states during one switching period. This maintains the six active states unchanged as in the traditional carrier based PWM. In simple boost control method is illustrated by two straight lines, which are employed to realize the shoot through duty ratio (Do). The first one is equal to the peak value of the three-phase sinusoidal reference Since Do = T_0/T, thus voltages while the other one is the negative of the first one.

Whenever the triangular carrier signal is higher than the positive straight line or lower than the negative straight line, the inverter will operate in shoot-through. Otherwise it works as a traditional PWM inverter. Since the value of the positive straight line equals to the maximum of the sinusoidal reference signals and the value of the negative straight line equals to the minimum of the sinusoidal reference signal, then the modulation index (M) and the shoot-through duty ratio (Do) are interdependent each other. It is also observed that shoot-through duty ratio (Do) decreases with increasing modulation index (M).

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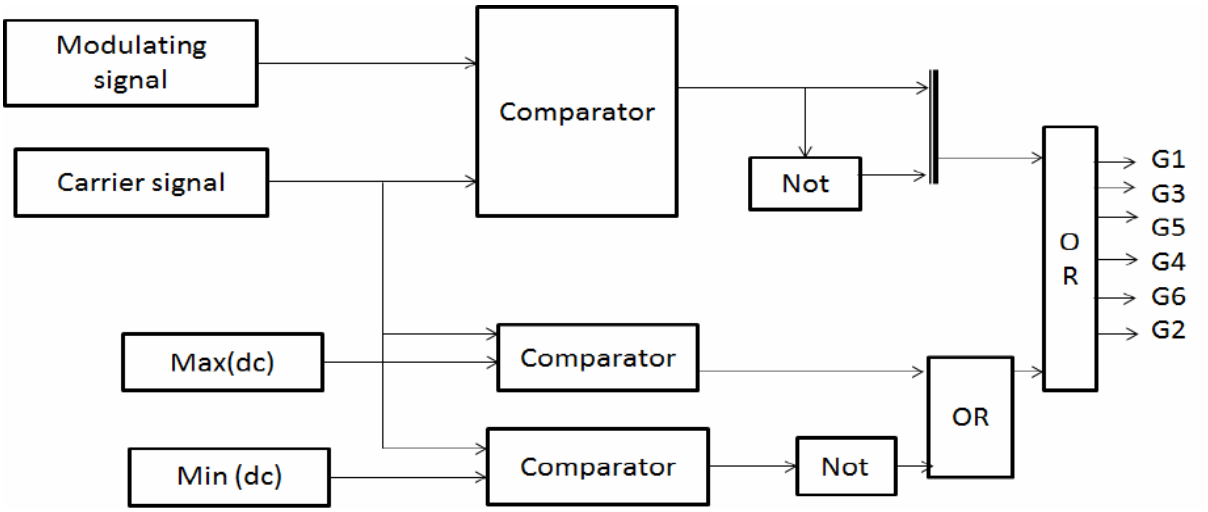

Implementation Diagram of SBC

Shoot-through pulses are inserted into the switching waveforms by logical OR gate. To produce switching pulses, three phase reference waveforms having peak value with modulation index (M) are compared with the same high frequency triangular signal. Comparator compares these two signals and produces pulses (when Vsin>Vtri, on and Vsin<Vtri, off). These pulses are then sent to gates of the power IGBT's through isolation and gate drive circuit. The pulse generation of the three phase leg switches (S1, S3 and S5-positive group/upper switches and S2, S4 and S6-negative group/lower switches).This method is much uncomplicated; however, the resulting voltage stress across the device is relatively high because some traditional zero states are not utilized either partially or fully. This characteristic will restrict the obtainable voltage gain because of the limitation of device voltage rating. For a complete switching period, Tis total switching period, T0is the zero state time period and Do is the shoot-through duty ratio. The control of ZSI is done by this control technique (SBC).

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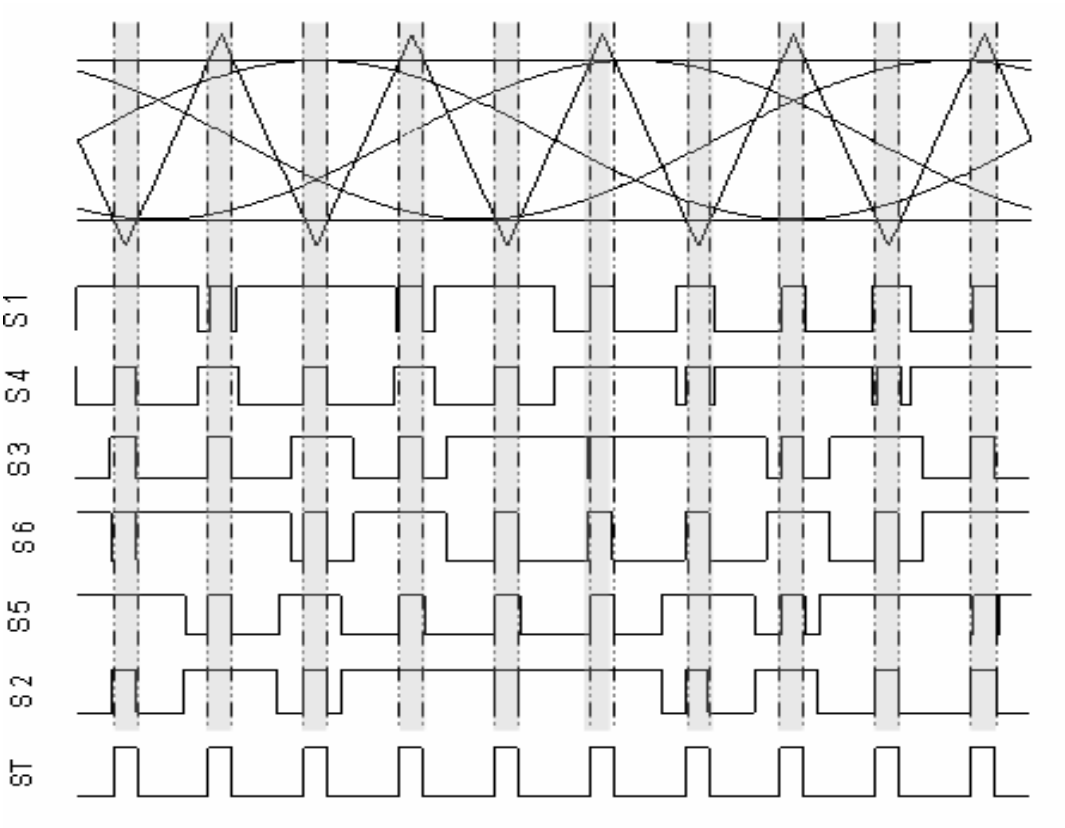
Theoretical Waveforms:



PWM Signals from Simple Boost Control

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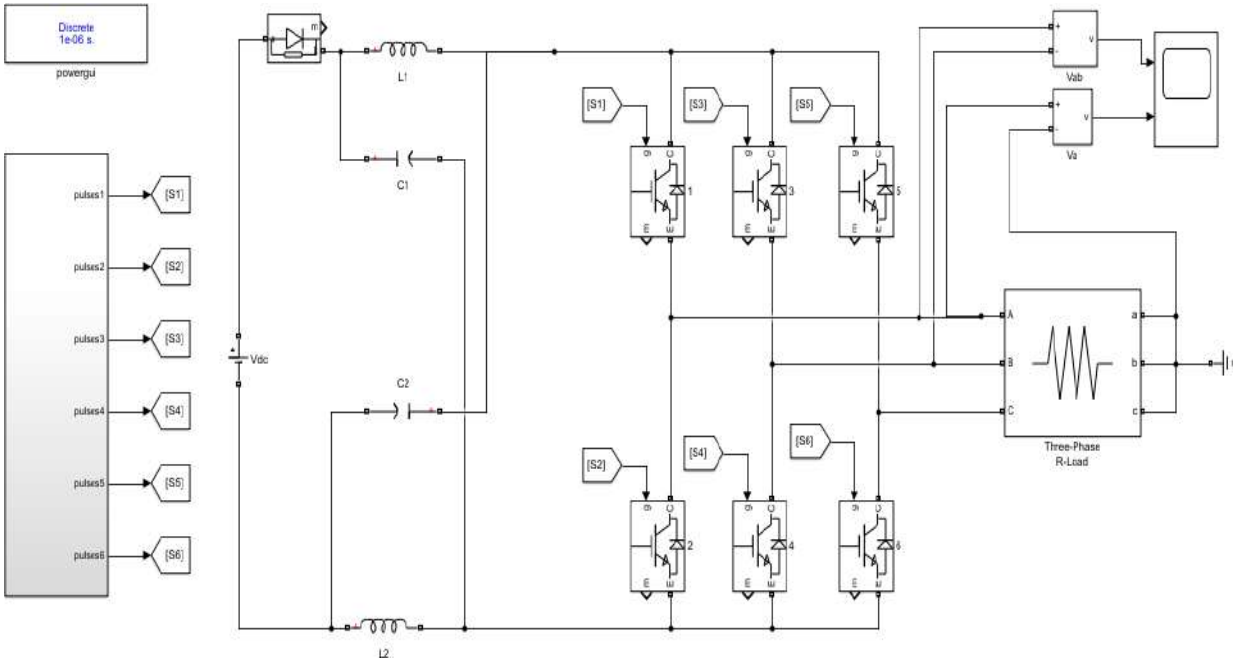
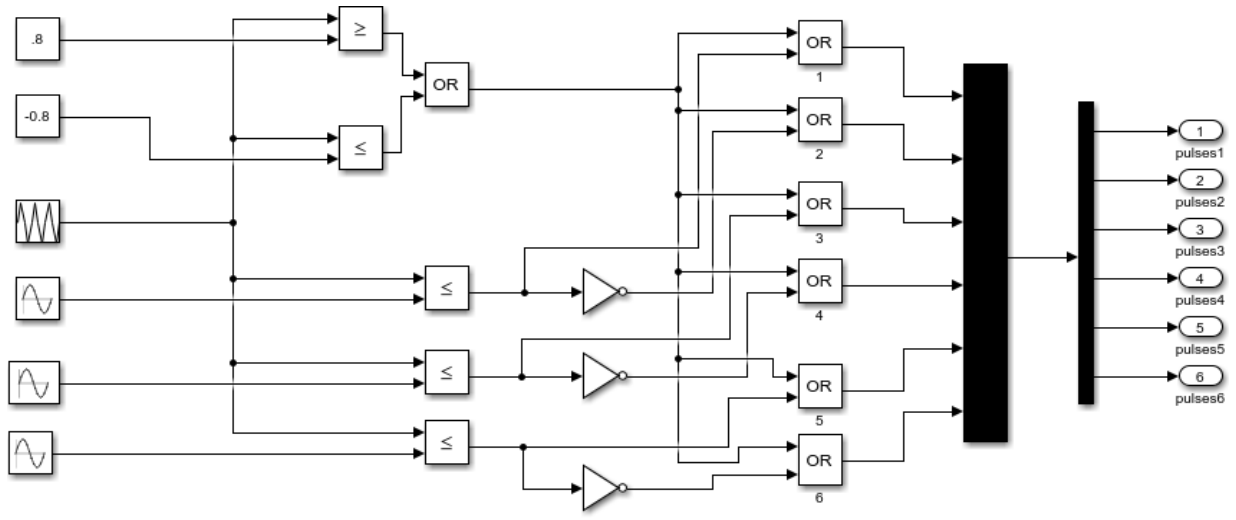
MATLAB/SIMULINK Circuit:



Z-Source Inverter



Z-Source Inverter PWM Generation

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Design Specifications:

Considering the Parameters for the given models followed as:

Input DC Voltage(Vdc)=250V

Supply Frequency (fs) = 50 Hz ,

Switching Frequency (fsw)= 10 KHz ,

Three Phase Resistive Load = 10 ohm per phase

In a Z-source Network: $L_1=L_2=160\mu H$ and $C_1=C_2=1000\mu F$

Modulation Index (M) = 0.8

Time Period (T)= 10^-5 Sec

Shoot Through Period (T_0) = 0.2*10^-5 Sec

Boost factor= $\frac{1}{1-2\frac{T_0}{T}}=1.66$

Output Voltage across Z-Source= M * B*Vdc= 0.8*1.66*250= 332V

Output across inverter= $M*B*\frac{V_{dc}}{2}=0.8*1.66*125=166V$

Procedure:

1. Rig up the circuit as per the circuit diagram in MATLAB/SIMULINK.
2. Observe the waveforms across the Z-source network, line voltage and phase voltages.

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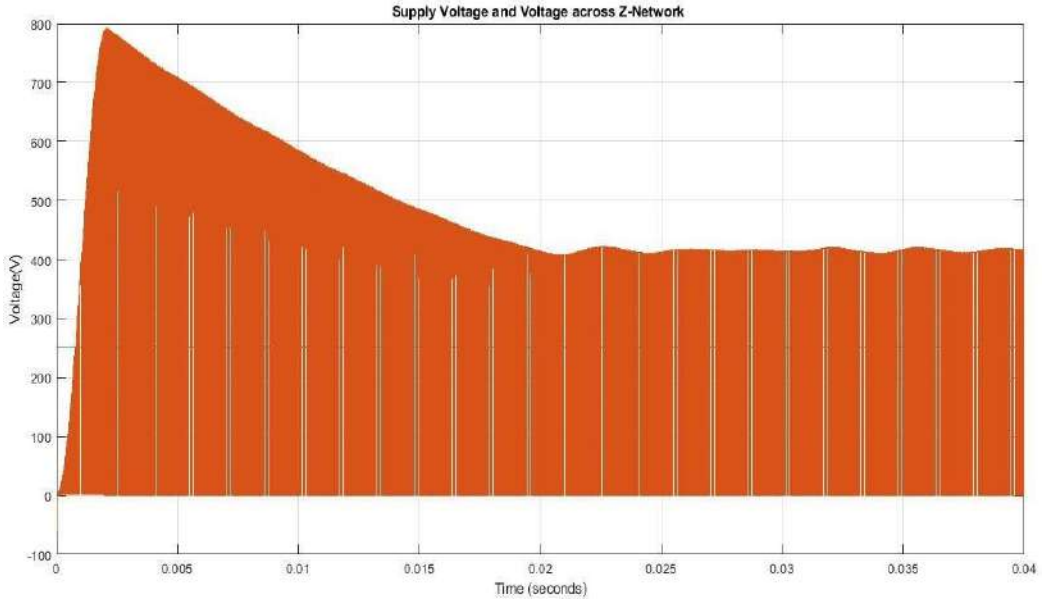
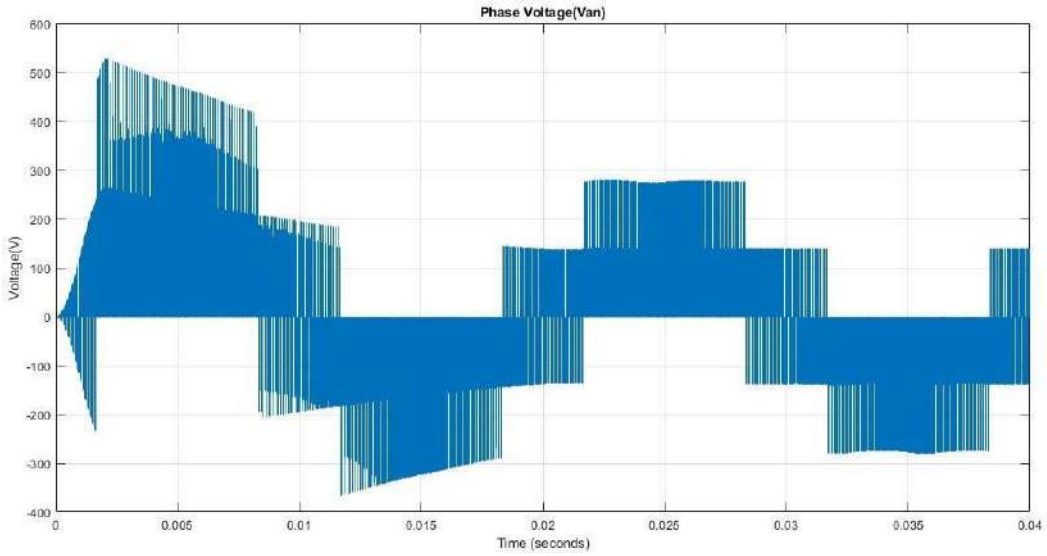
Simulation Waveforms:



Supply Voltage and Voltage across the Z-Source netwok



Phase Voltage (Van)

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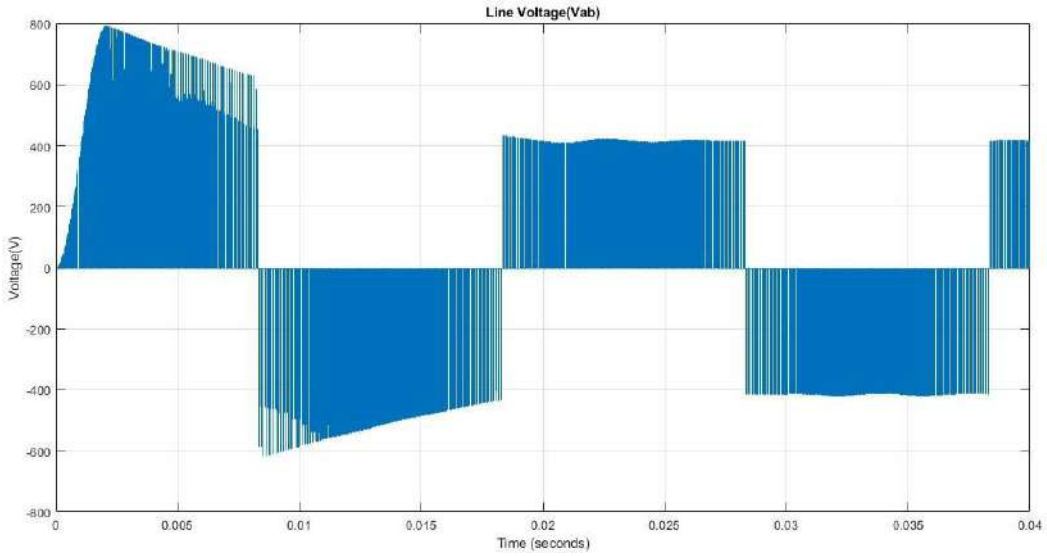

Line Voltage (Vab)

Result: Z-Source Inverter is simulated using MATLAB/SIMULINK and its operation is studied using various waveforms.

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THREE LEVEL DIODE CLAMPED INVERTER

Aim: Simulation of Three Level Diode Clamped Inverter using PWM Technique.

Circuit Diagram:

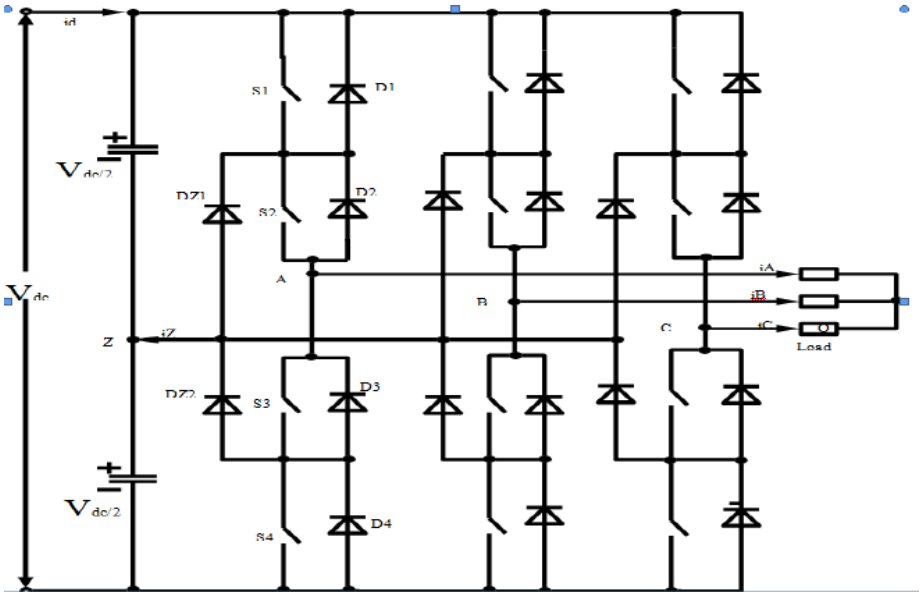
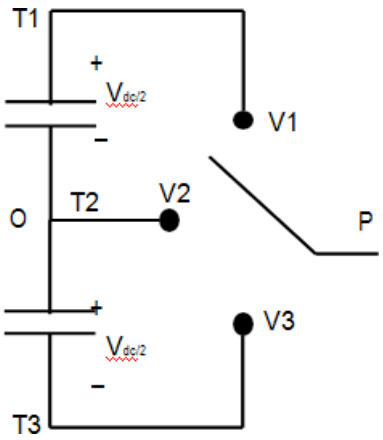


Fig.1. Circuit Diagram of 3 level diode clamped inverter

Basic operation of 3 level Diode Clamped inverter:



When P is connected to T1 the Vpo= +Vdc/2

When P is connected to T2 the Vpo=0

When P is connected to T3 the Vpo= -Vdc/2.

From the above figures, it is clear that in between P and O voltage is present. So to lock the voltages (+Vdc , -Vdc) clamping diodes are required.

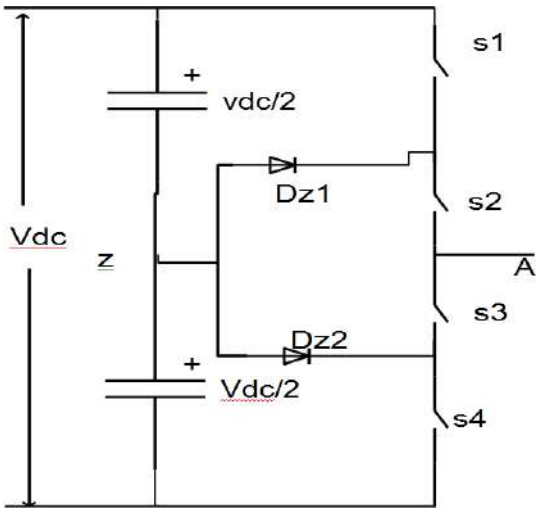


Fig.2 Circuit diagram of 3 Level diode clamped multilevel inverter for one leg (Phase A)

Operation of Switches:

S1	S2	S3	S4	Inverter Terminal voltage
ON	ON	OFF	OFF	+Vdc/2
OFF	ON	ON	OFF	0
OFF	OFF	ON	ON	-Vdc/2

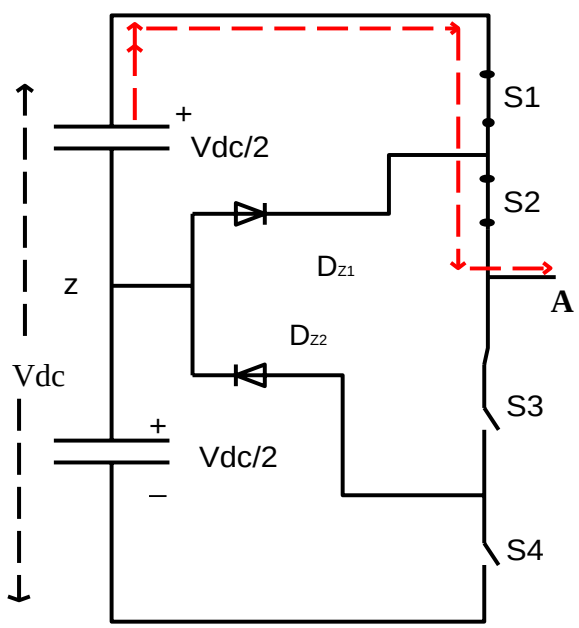


Fig.3 MODE1- S1, S2 'ON'

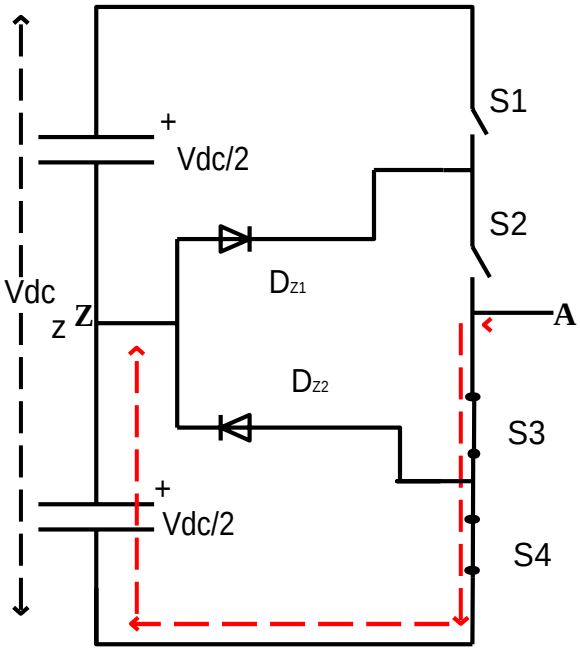


Fig.4 MODE 2 - S3, S4 'ON'

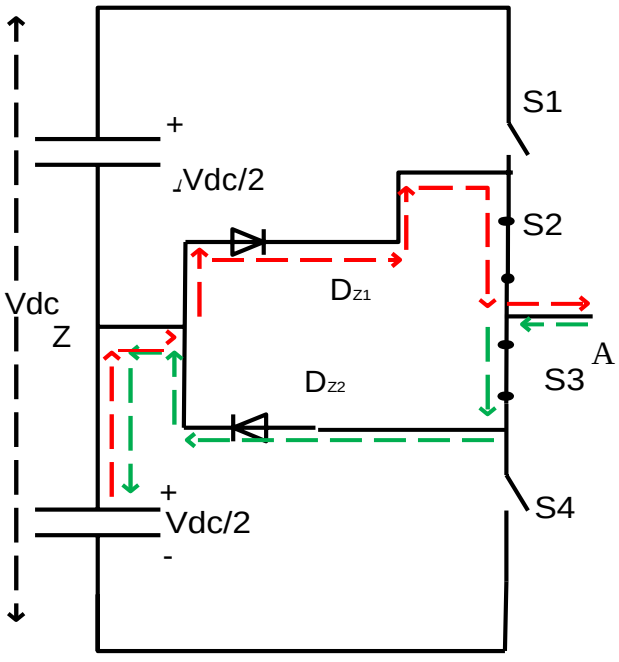


Fig.5 MODE3 S2 (OR) S3 ' ON'

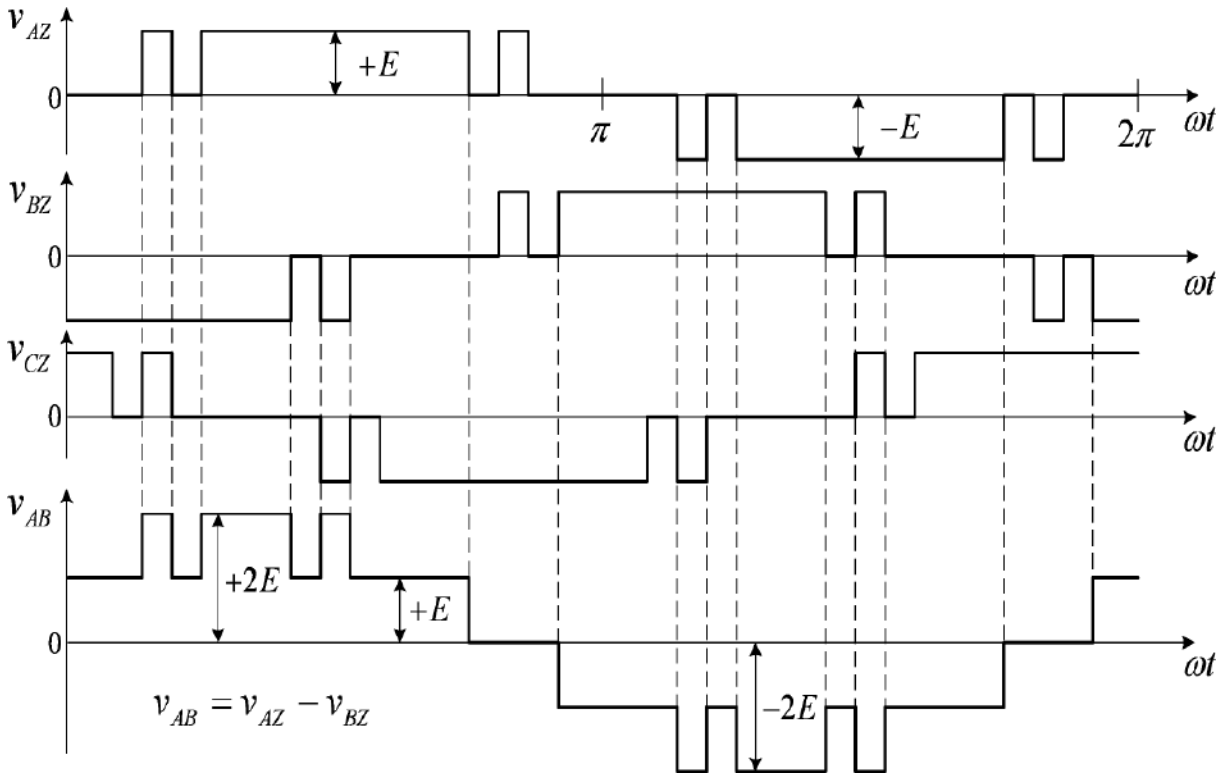


Fig .6 Phase and Line voltage waveforms

Note: Consider E=Vdc/2 and –E= -

Vdc/2 **Phase disposition Technique:**

The rules for phase disposition method for a three level inverter are:

1) Two carrier waveforms are arranged in phase.
2) The converter is switched to + Vdc / 2 when the sine wave is greater than both carrier waveforms.
3) The converter is switched to zero when sine wave is lower than upper carrier wave but is higher than the lower carrier wave.
4) The converter is switched to - Vdc / 2 when the sine wave is less than both carrier waveforms.

In the PWM scheme, there are two triangular waves, the upper triangle ranges from 1 to 0 and the lower triangle ranges from 0 to –1. During the positive cycle of the reference signal, when the reference wave is greater than triangle 1 and triangle 2, S1 and S2 are turned ON. When S1 and S2 are turned ON, the converter switches to + Vdc / 2 and when S2 and S3 are ON, the converter switches to zero and hence during the entire positive cycle S2 is completely turned ON and S1 and S3 will be turning ON and OFF. Thus, the converter output voltage switches from + Vdc / 2 to 0. During the negative half cycle of the modulation signal the converter output voltage switches from 0 to -Vdc / 2.

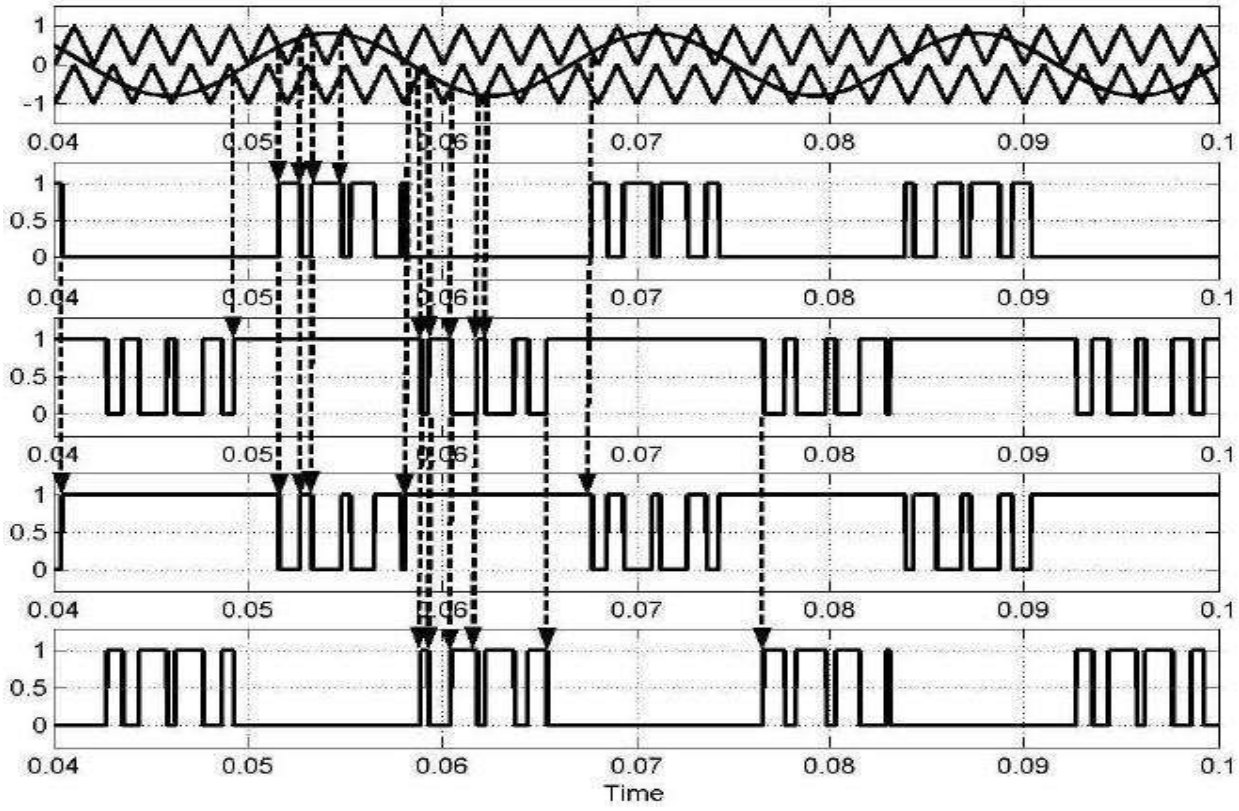


Fig.7 Switching pattern produced using the PD carrier-based PWM scheme.

(a) Carrier and the modulation signals (b) S1 (c) S2 (d) S3 (e) S4.

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Design Considerations:

+Vdc/2=50 Volts, -Vdc/2= -50 volts, R=10 Ohms , PWM = Phase Disposition method.

Procedure:

1. Rig up the circuit as per the diagram.
2. To generate PWM, one Reference wave and two Carrier waves must be considered.
3. The carrier wave must be triangular wave and linear modulation is considered.
4. For linear modulation M.I is less than 1 and hence the reference magnitude is considered to be less than carrier wave magnitude.
5. The reference wave frequency is 50Hz and carrier wave frequency is considered as per requirement.
6. Run the simulation and save the waveforms in workspace.

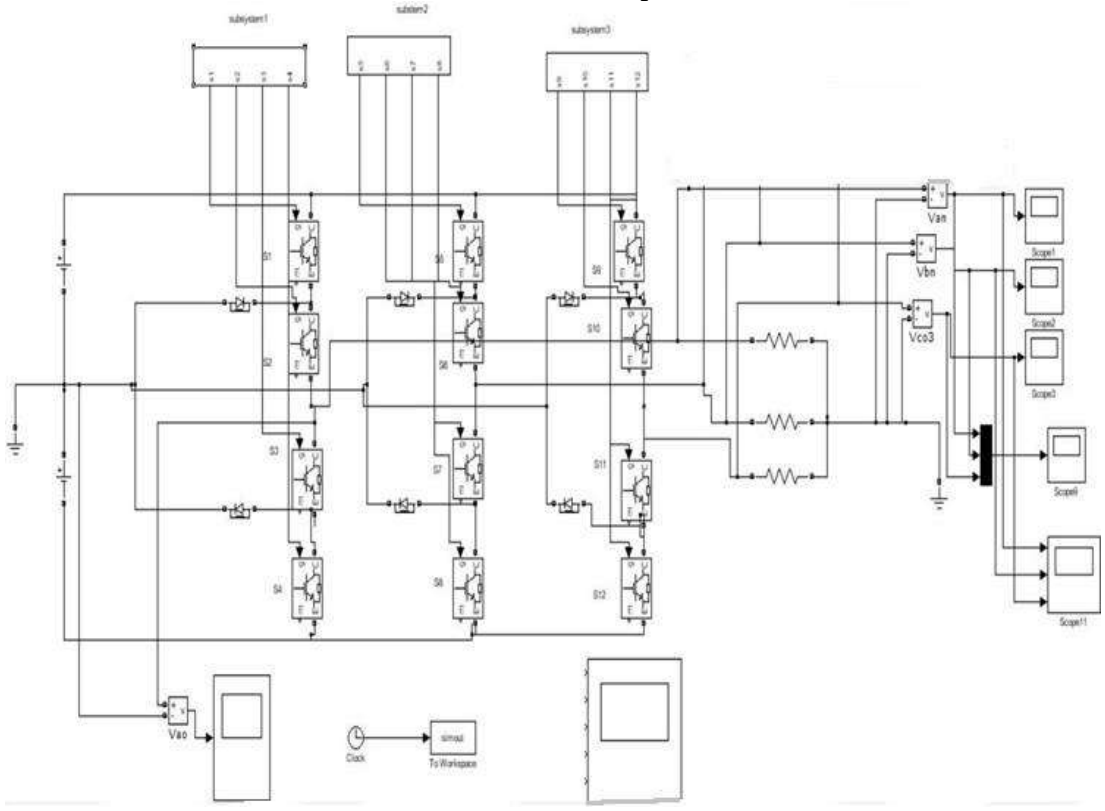


Fig. 8 Simulink diagram of three level Diode Clamped inverter

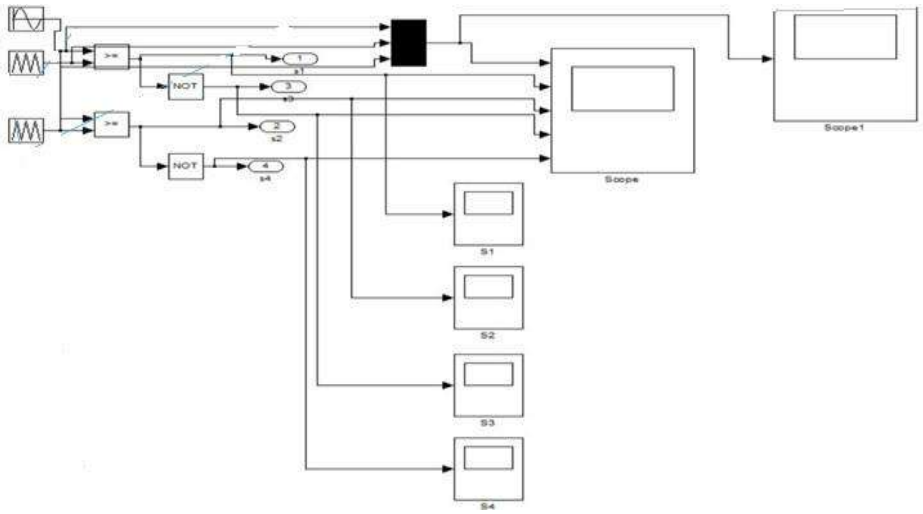
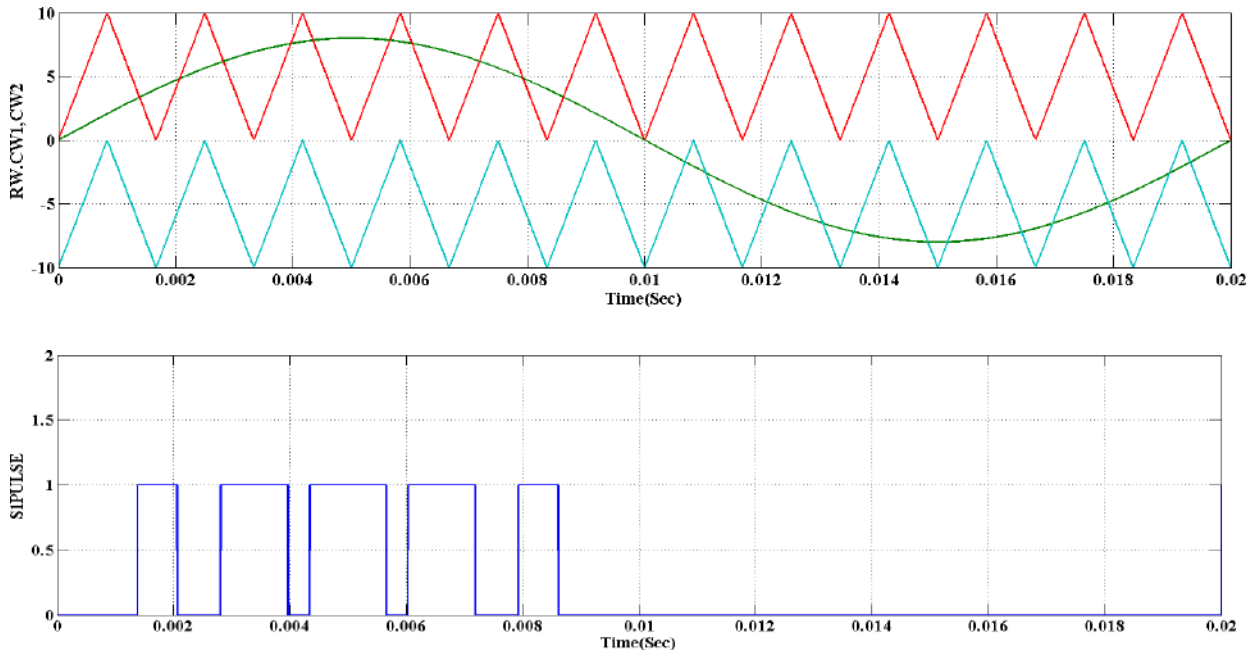


Fig. 9 PWM signal generation



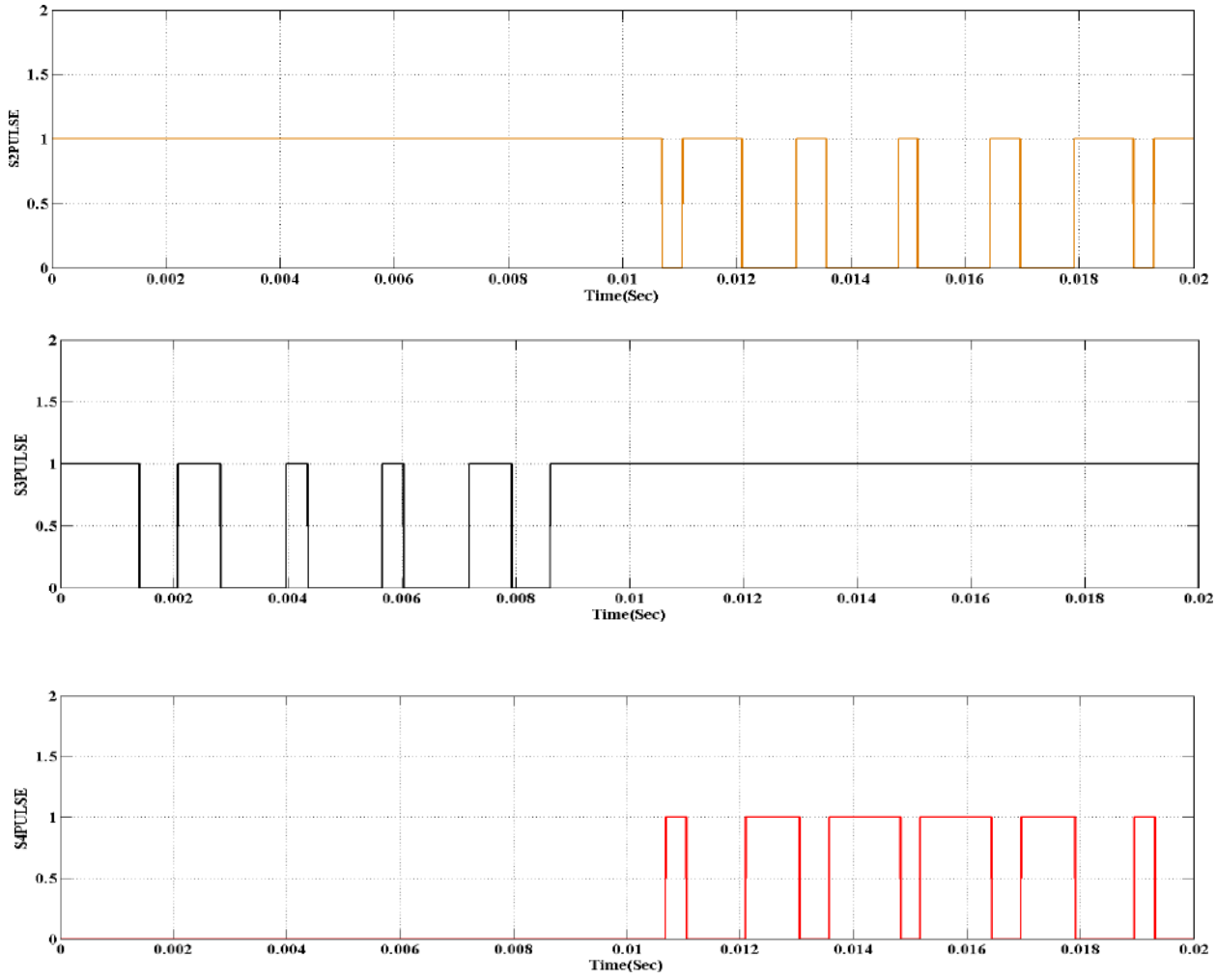


Fig.10 Gate pulses for PHASE A

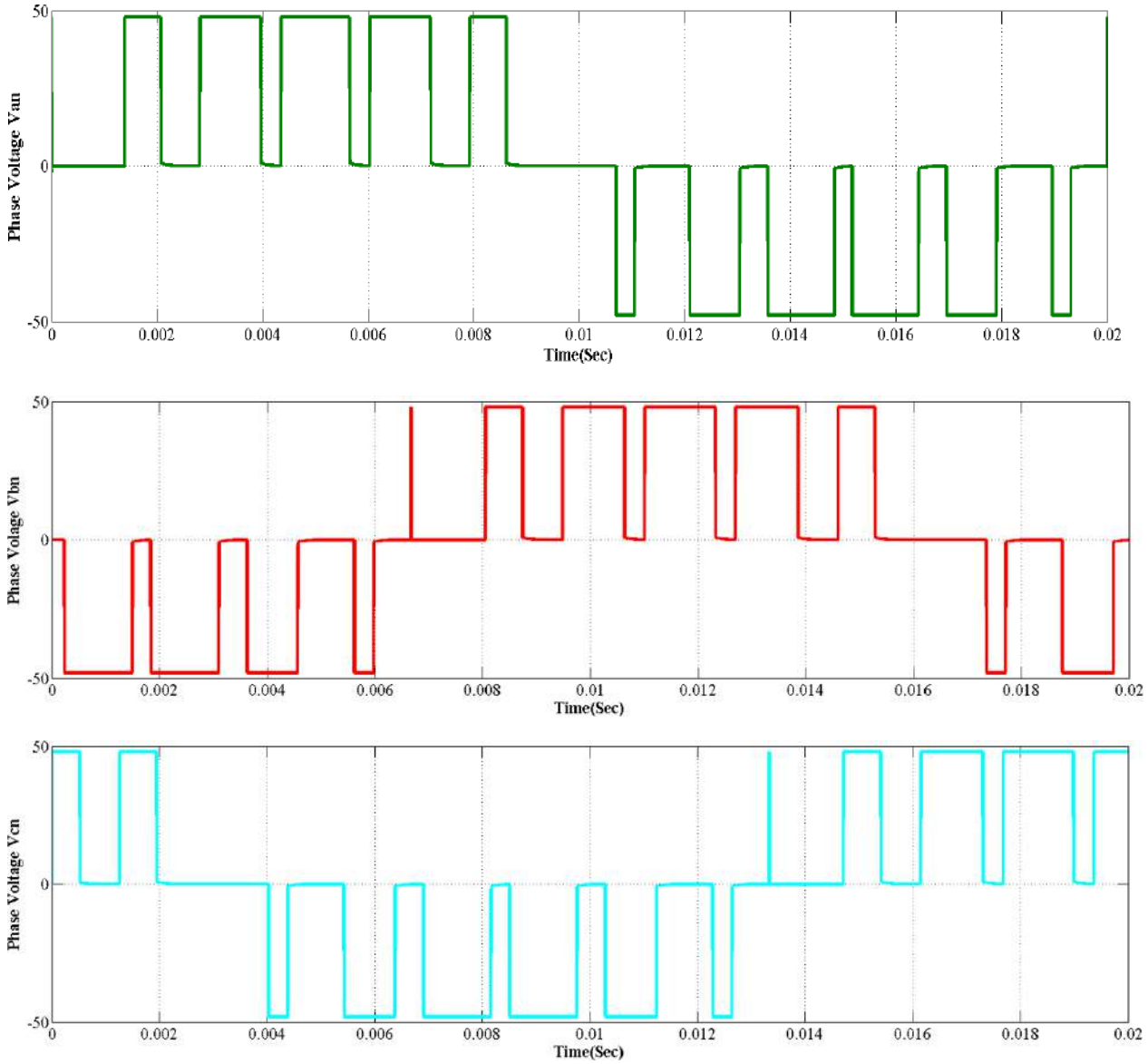


Fig. 11 Phase voltages of 3 phase 3 level diode clamped multilevel inverter

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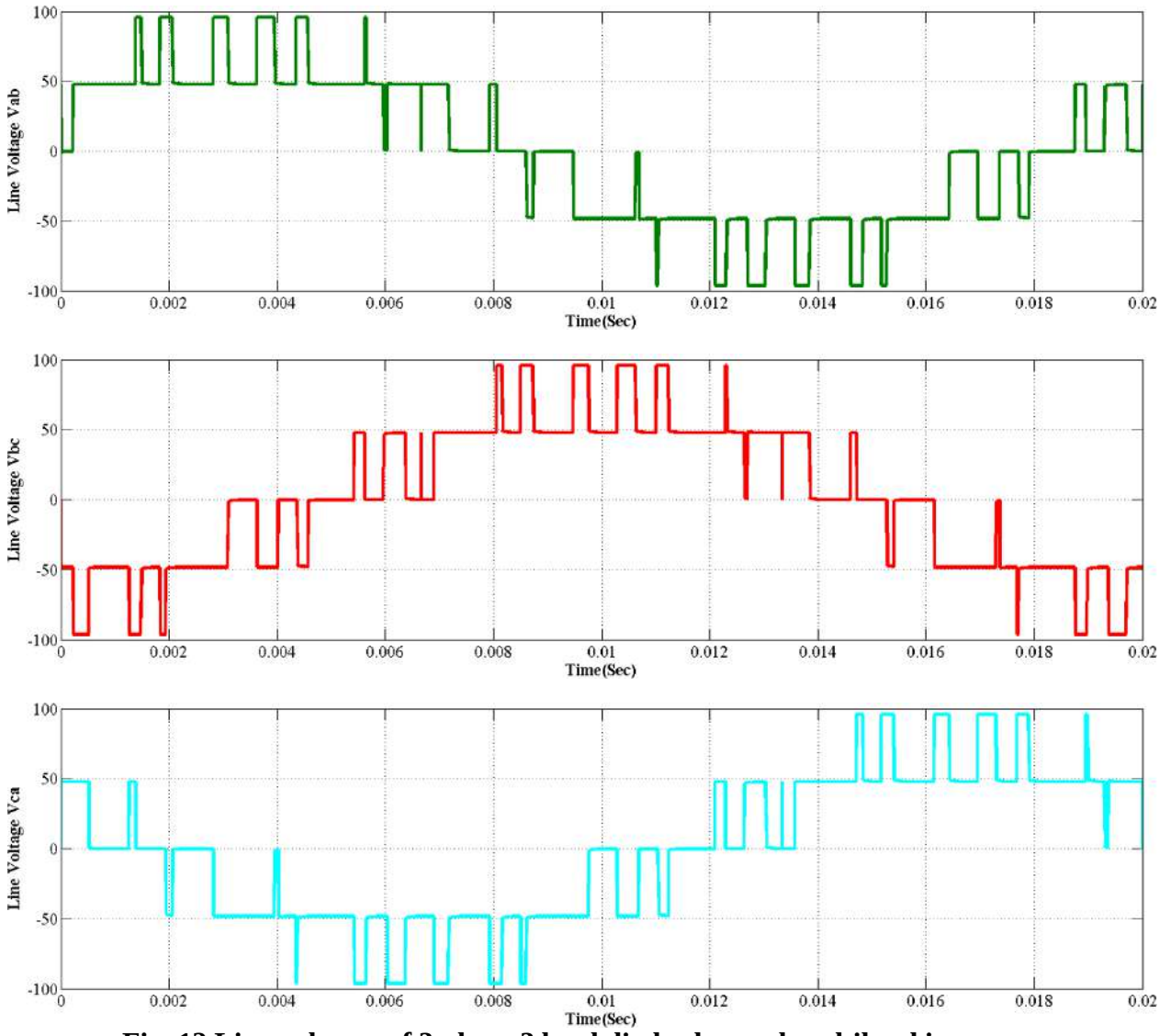

Fig. 12 Line voltages of 3 phase 3 level diode clamped multilevel inverter

Result : The three level Diode Clamped inverter is simulated using MATLAB/SIMULINK and its operation is studied using various waveforms.

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FIVE LEVEL DIODE CLAMPED INVERTER

Aim: Simulation of Five Level Diode Clamped Inverter using PWM Technique.

Circuit Diagram:

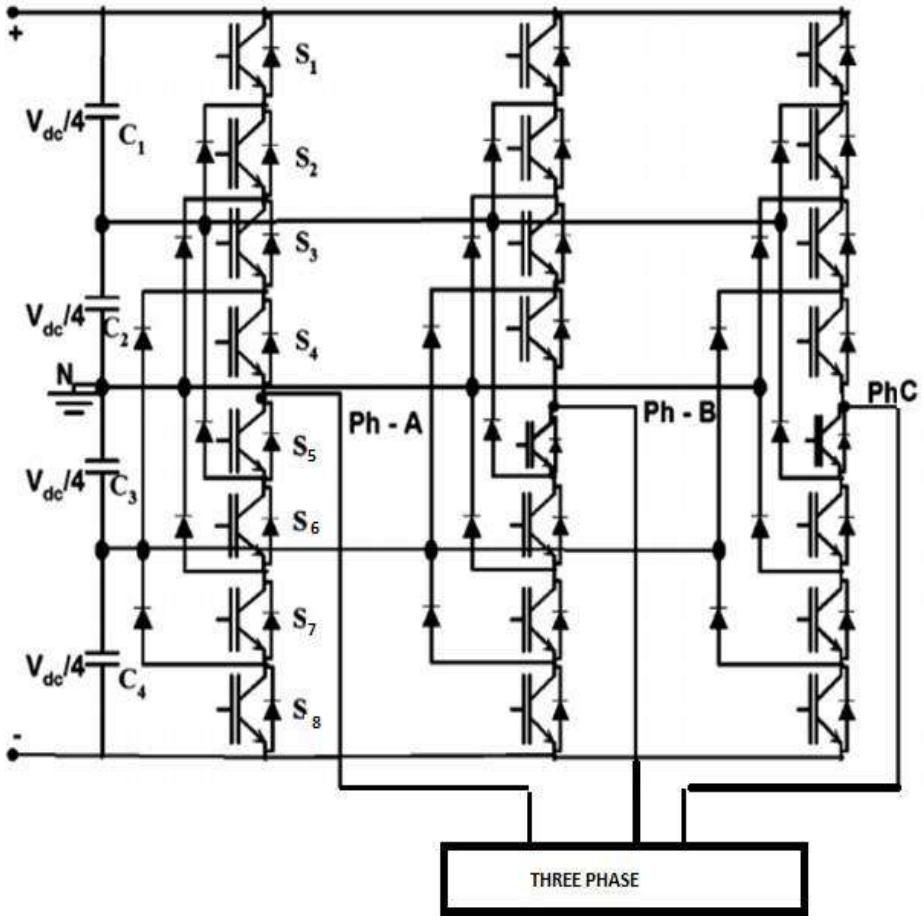

Fig.1. Circuit Diagram of 5 level diode clamped inverter

Operation of Switches:

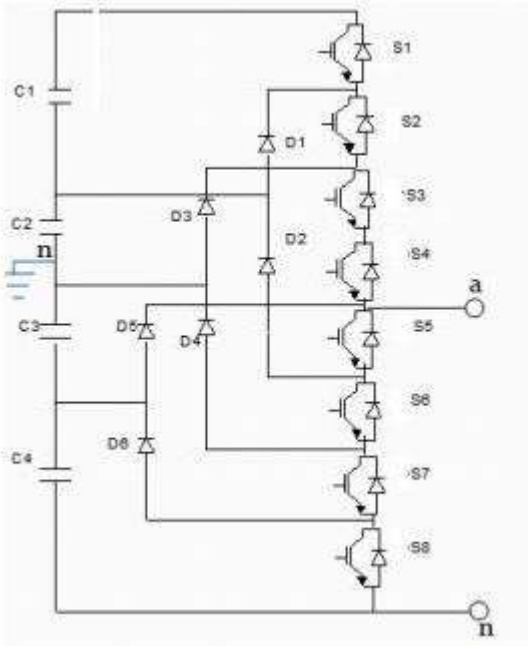

Fig.2 Circuit diagram of 5 Level diode clamped multilevel inverter for one leg (Phase A)

Output Voltage Va0	Switch State							
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
Vdc/2	1	1	1	1	0	0	0	0
Vdc/4	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
-Vdc/4	0	0	0	1	1	1	1	0
Vdc/2	0	0	0	0	1	1	1	1

In- Phase disposition Technique:

The rules for In- phase disposition method for a five level inverter are:

1) Four carrier waveforms are arranged in phase and are compared with sinusoidal reference waveform.
2) The converter is switched to + Vdc / 2 when the sine wave is greater than both upper carrier waveforms.
3) The converter is switched to + Vdc / 4 when sine wave is lower than upper carrier wave but is higher than all other carrier waves.
4) The converter is switched to 0 when the sine wave is lower than upper carrier waves but higher than lower carrier waveforms.
5) The converter is switched to –Vdc/4 when sine wave is higher than lower most carrier wave and lesser than all other carrier waves.
6) The converter is switched to - Vdc / 2 when the sine wave is less than both carrier waveforms.

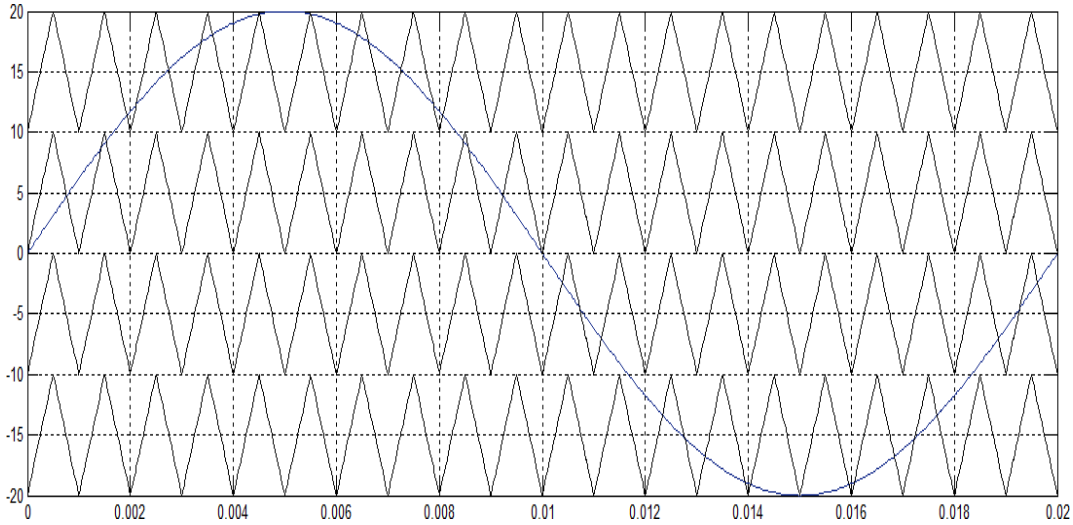

Fig.3 PD carrier-based PWM scheme (Carrier and the modulation signals)

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Design Considerations:

$+V_{dc/4}$=50 Volts, $V_{dc/2}$= 100 volts, R=10 Ohms , PWM = Phase Disposition method, MI = 0.8 , Ref wave amp = 20V.

Procedure:

1. Rig up the circuit as per the diagram.
2. To generate PWM, one Reference wave and four Carrier waves must be considered.
3. The carrier wave must be triangular wave and linear modulation is considered.
4. For linear modulation M.I is less than 1 and hence the reference magnitude is considered to be less than carrier wave magnitude.
5. The reference wave frequency is 50Hz and carrier wave frequency is considered as 1000Hz.
6. Run the simulation and save the waveforms in workspace.

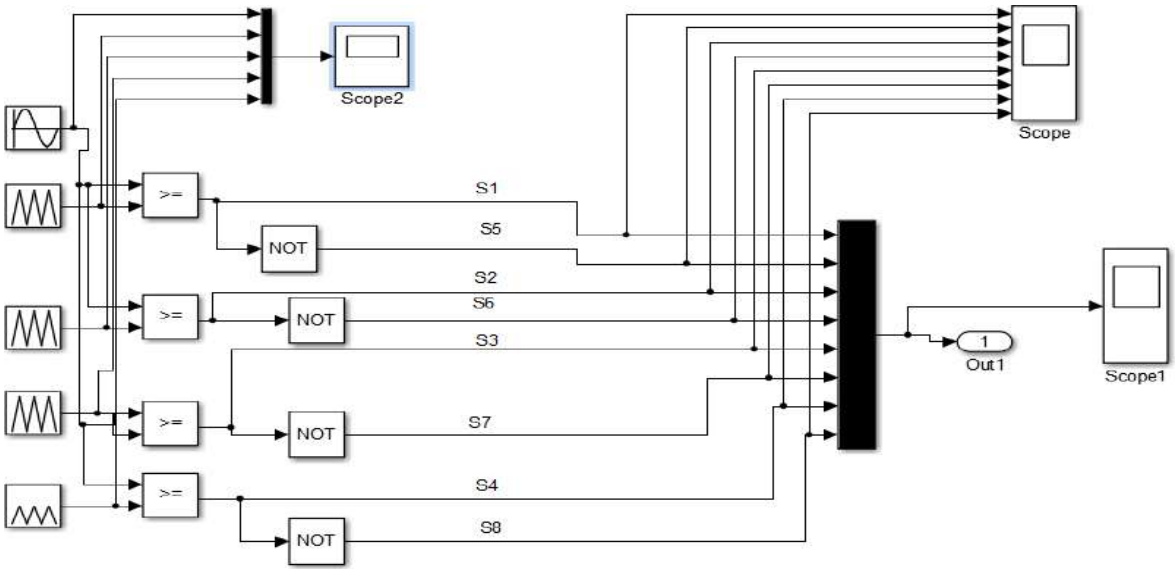

Fig. 4 Pulse Generation

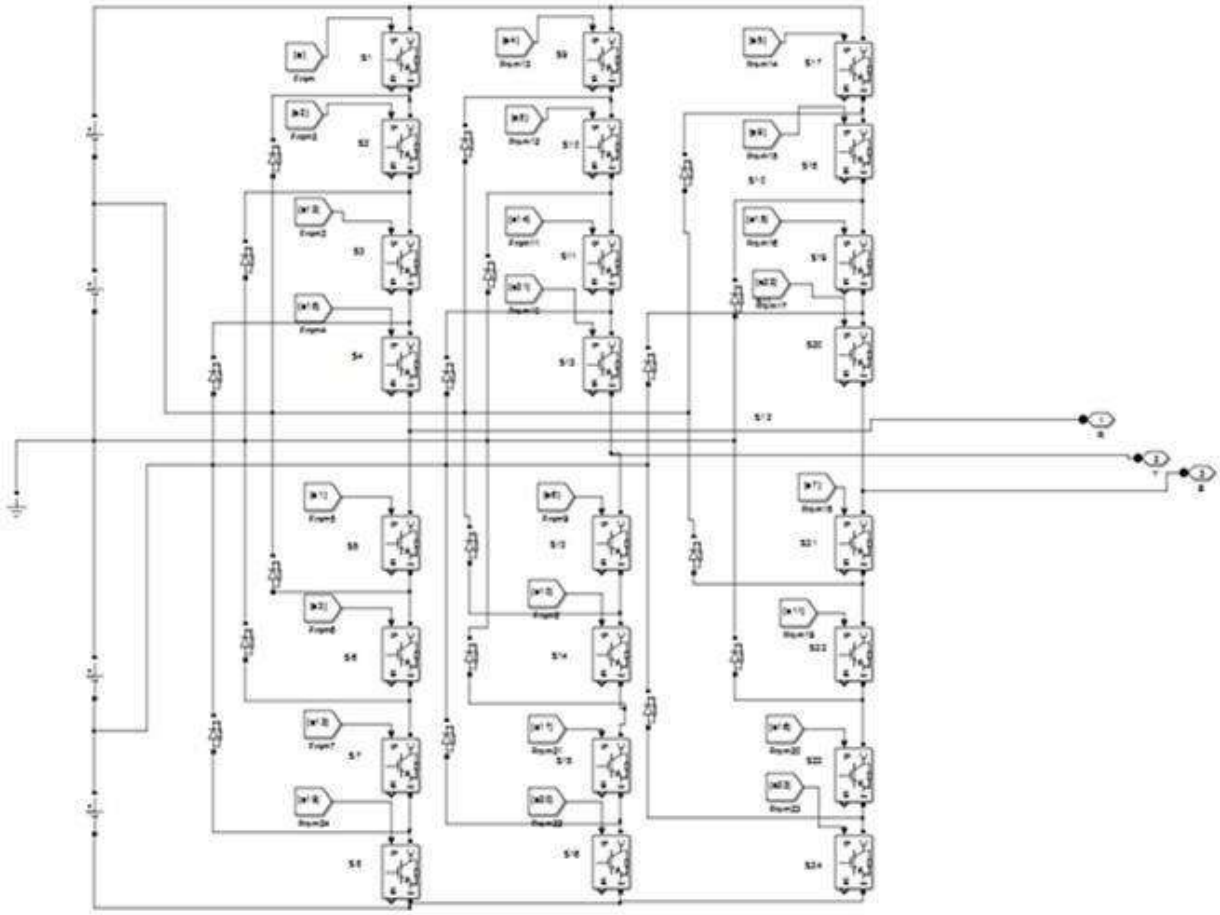

Fig. 5 Simulink Diagram of five level diode clamped inverter

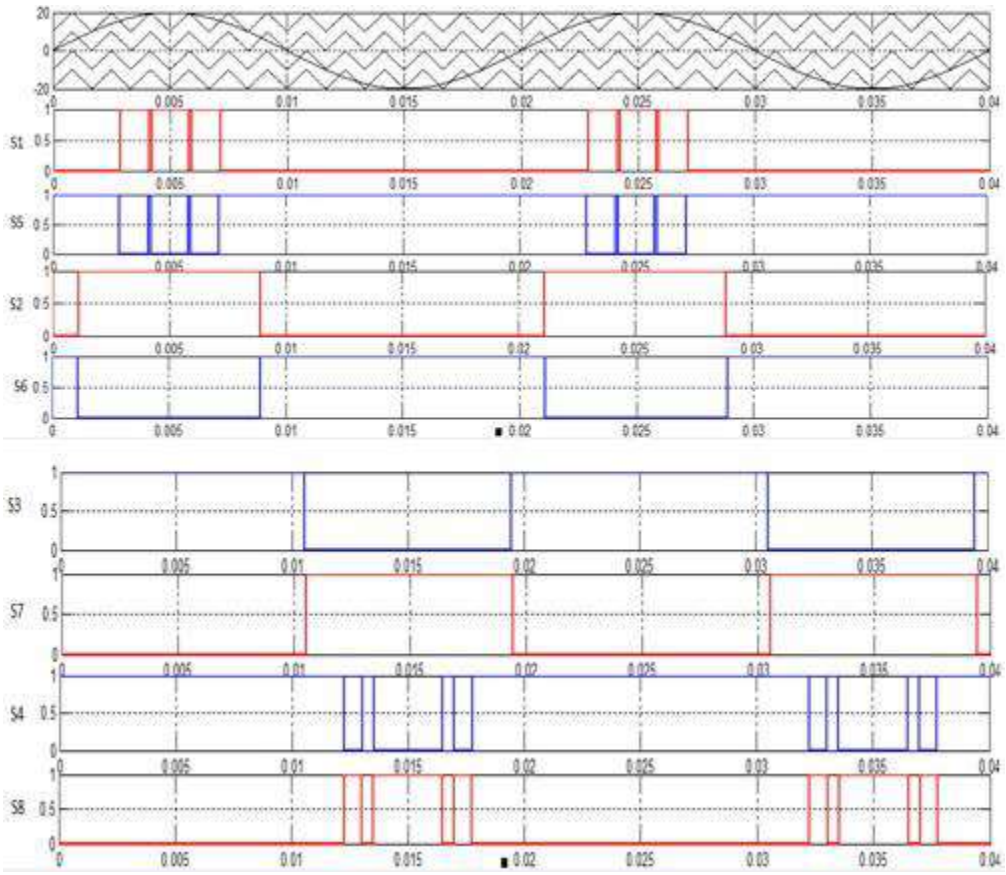

Fig. 6 Switching pulses to the switches of Phase A

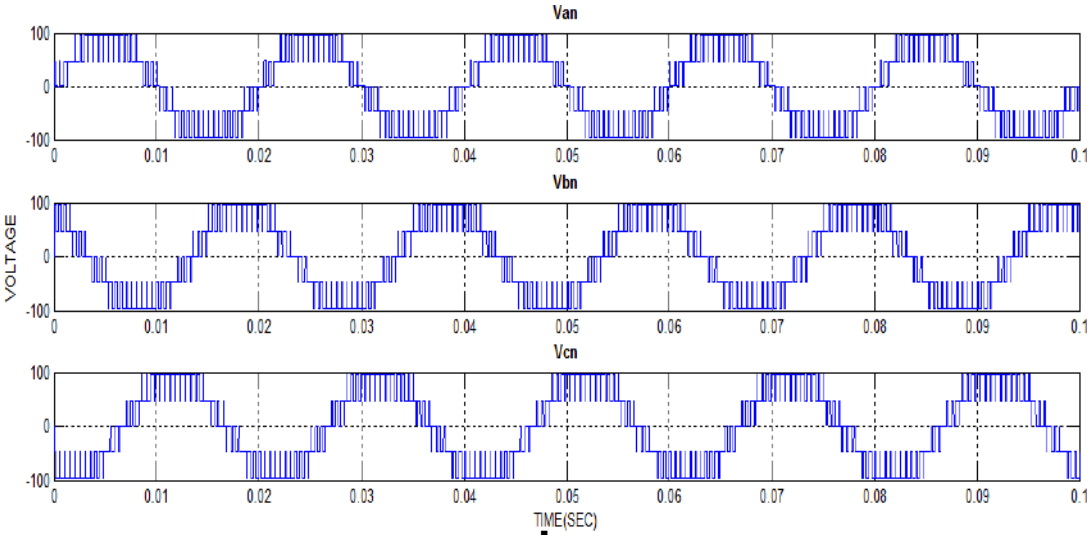

Fig.7 Phase voltages of the inverter output voltage

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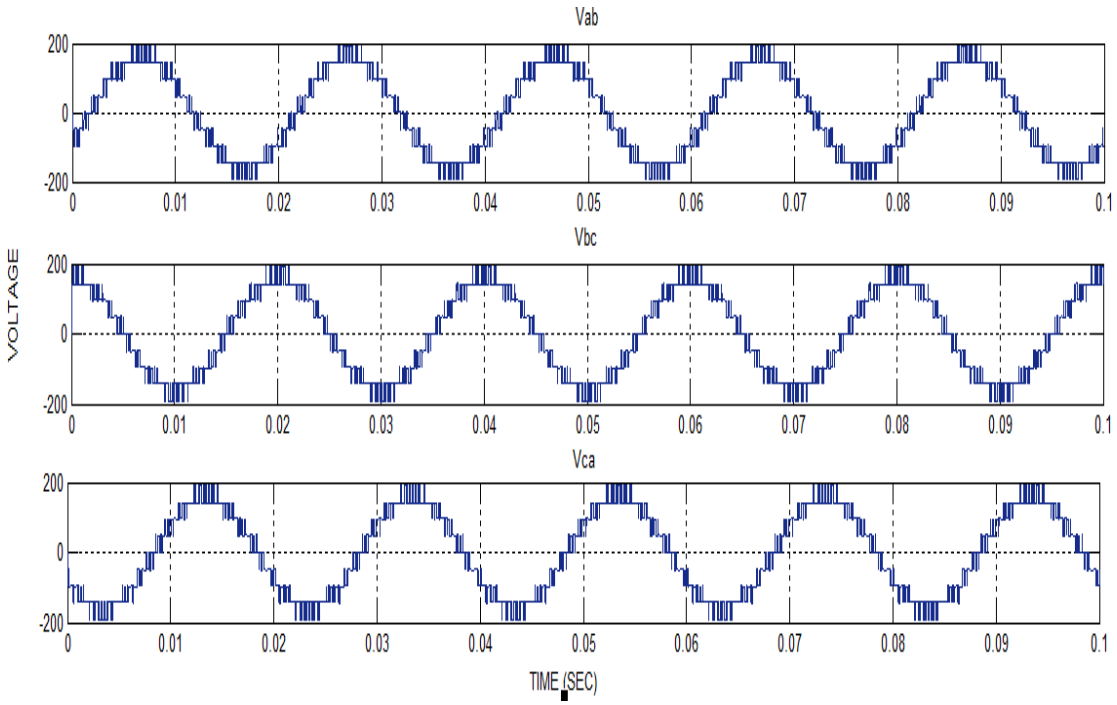

Fig.8 Line voltages of the inverter output voltage

Result : The five level Diode Clamped inverter is simulated using MATLAB/SIMULINK and its operation is studied using various waveforms.

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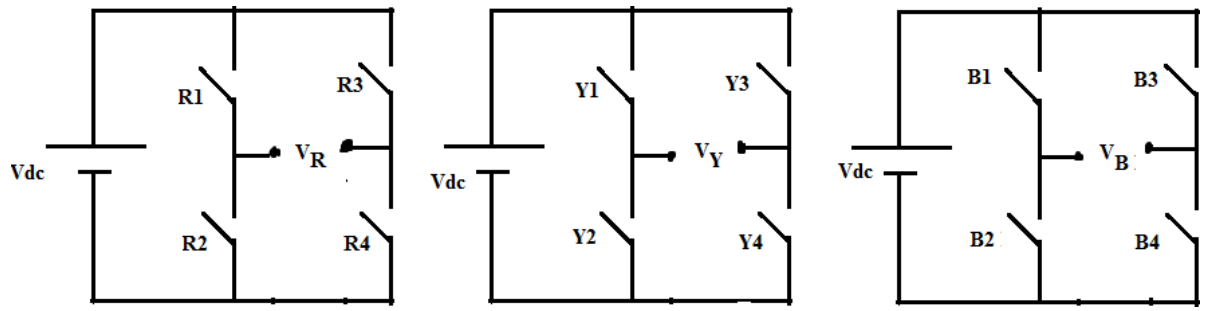
THREE PHASE THREE LEVEL SINUSOIDAL PWM BASED H-BRIDGE INVERTER

Aim: To study the three phase 3-level h-bride Inverter with R-Load using MATLAB / SIMULINK software.

Circuit Diagram:



Theory:

A cascaded multilevel inverter consists of a series of H-bridge (single-phase, full-bridge) inverter units. The general function of this multilevel inverter is to synthesize a desired voltage from several separate dc sources, which may be obtained from batteries, fuel cells, or solar cells. The ac terminal voltages of different level inverters are connected in series.

The output of each bridge could be summed up to generate almost sinusoidal output voltage waveform for nth level of CHMI each full bridge inverter unit forming the CHMI with separate dc. Four semiconductors switches are able to produce three different voltage levels namely +Vdc, 0 and –Vdc depending on the switching state. Each of the switching always conducts for 180 degree or half-cycle regardless of the pulse width of the quasi-square wave so that this method will result in the equalization of the current stress in each of the components.

Each H-bridge was activated at certain amount of time at different start up angle and because each bridge was fed by separate dc source, the output of all the bridge which formed the CHMI output would be the sum of the separated dc sources for three phase nth level of CHMI inverter.

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Modulation Techniques

In terms of the control strategy of a multilevel inverter, numerous researchers in the power electronic field have developed many modulation techniques. The two famous and simple modulation techniques are the Sinusoidal Pulse Width Modulation (SPWM) and, the Space Vector Pulse Width Modulation (SVPWM). A multilevel inverter switching signal can be generated using these two methods with less switching losses and harmonic distortion.

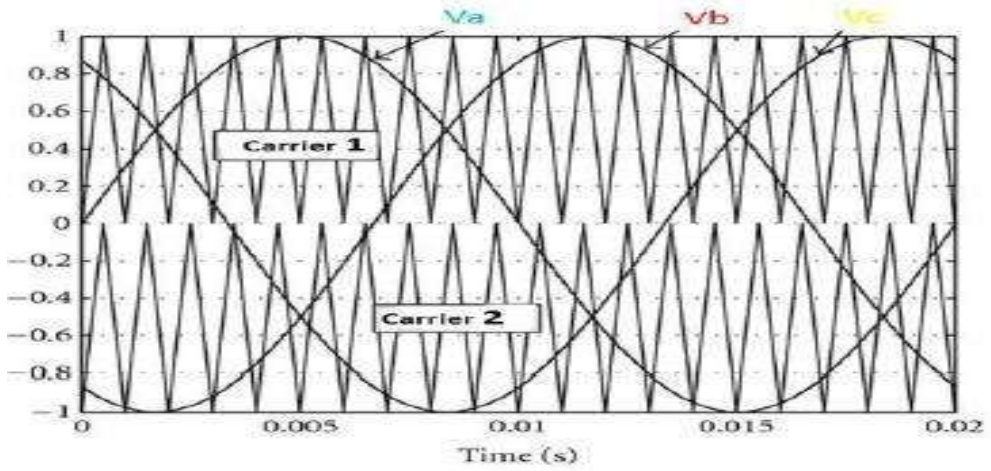
Sinusoidal Pulse Width Modulation (SPWM)

The CHMI was controlled by the SPWM where sinusoidal wave was compared with square waves to generate the switching signal that would trigger the semiconductors switches in time sequence considering the phase between the phases shift three phase inverter legs. This method used N-1 level carrier signals to generate the N-level inverter output voltage.

To generate the switching pulses of 3-level inverter utilizing sinusoidal pulse width modulation, two carrier signals were compared with one reference sine wave where the amplitude of the carrier signal was dividedinto two regions to fit the reference sine wave amplitude.

$$\text{Modulation Index (M)} = \frac{V_r}{V_c}$$

Theoretical Waveforms:



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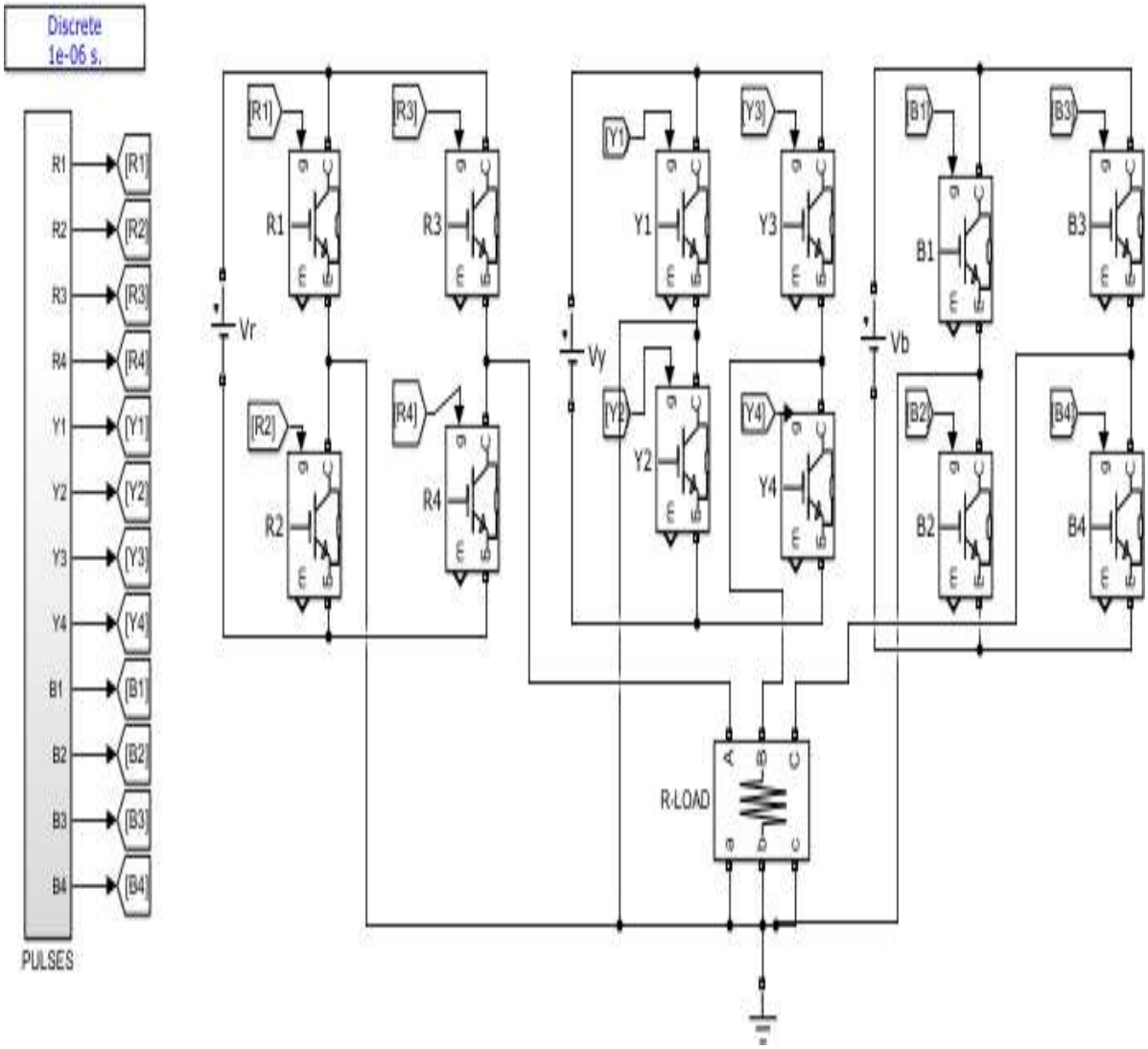
MATLAB/SIMULINK Circuit:



Three Phase Three-Level H-Bridge Inverter

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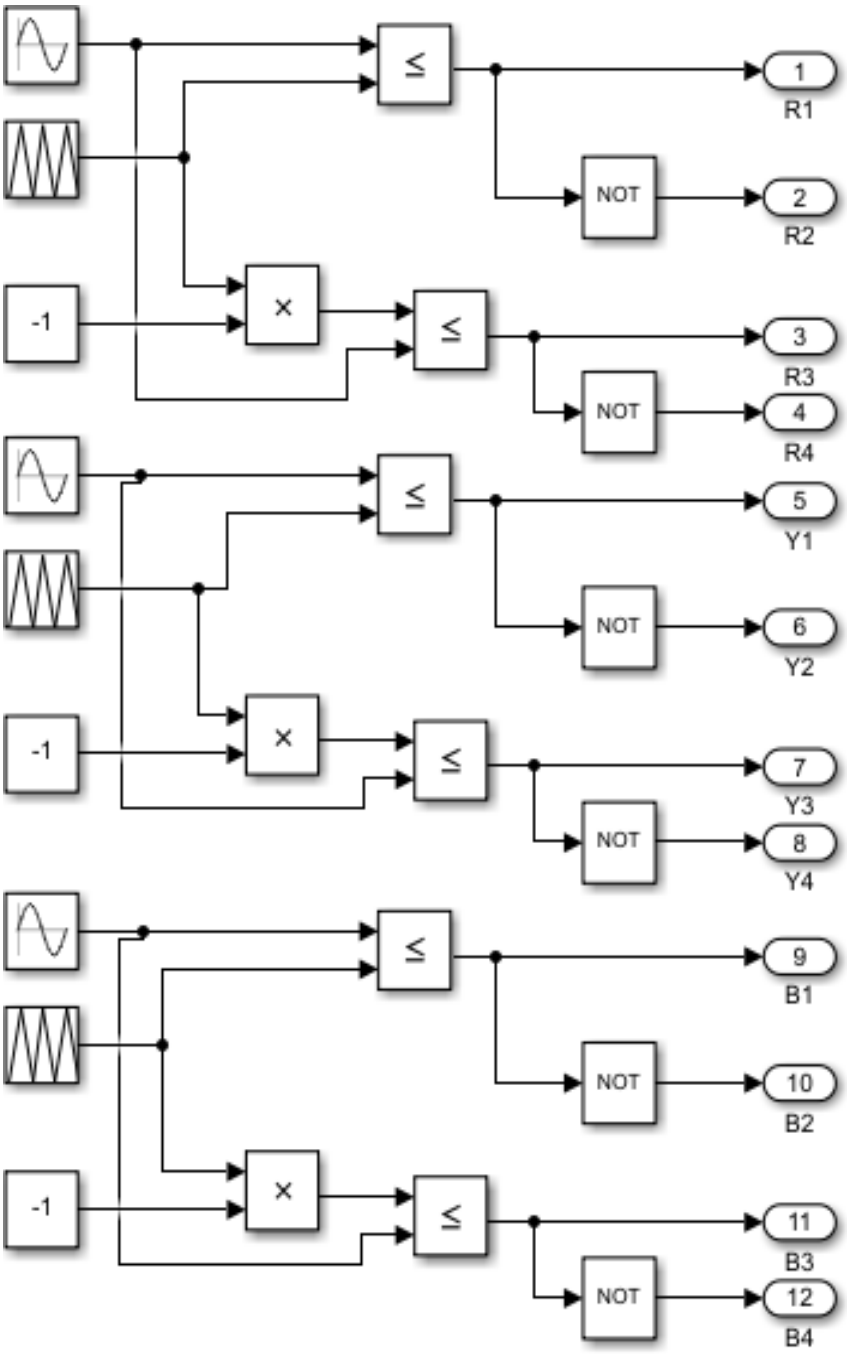

3-Phase 3-Level H-bridge Sinusoidal PWM Generation

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Design Specifications:

Considering the Parameters for the given models followed as:

Input DC Voltage(Vdc)=250V

Supply Frequency (f) = 50 Hz,

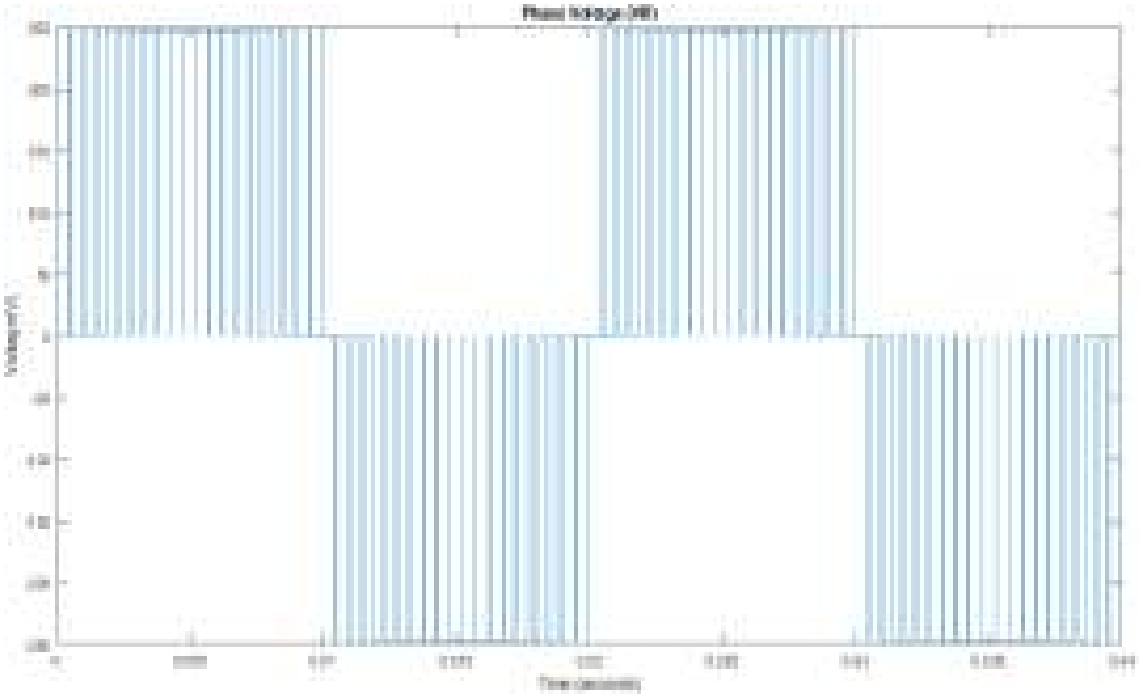
Switching Frequency = 1kHz,

Three Phase Resistive Load = 10 ohm per phase

Procedure:

1. Rig up the circuit as per the circuit diagram in MATLAB/SIMULINK Model platform.
2. Observe the output phase and line voltages.

Simulation Waveforms:



Phase Voltage (V_R)

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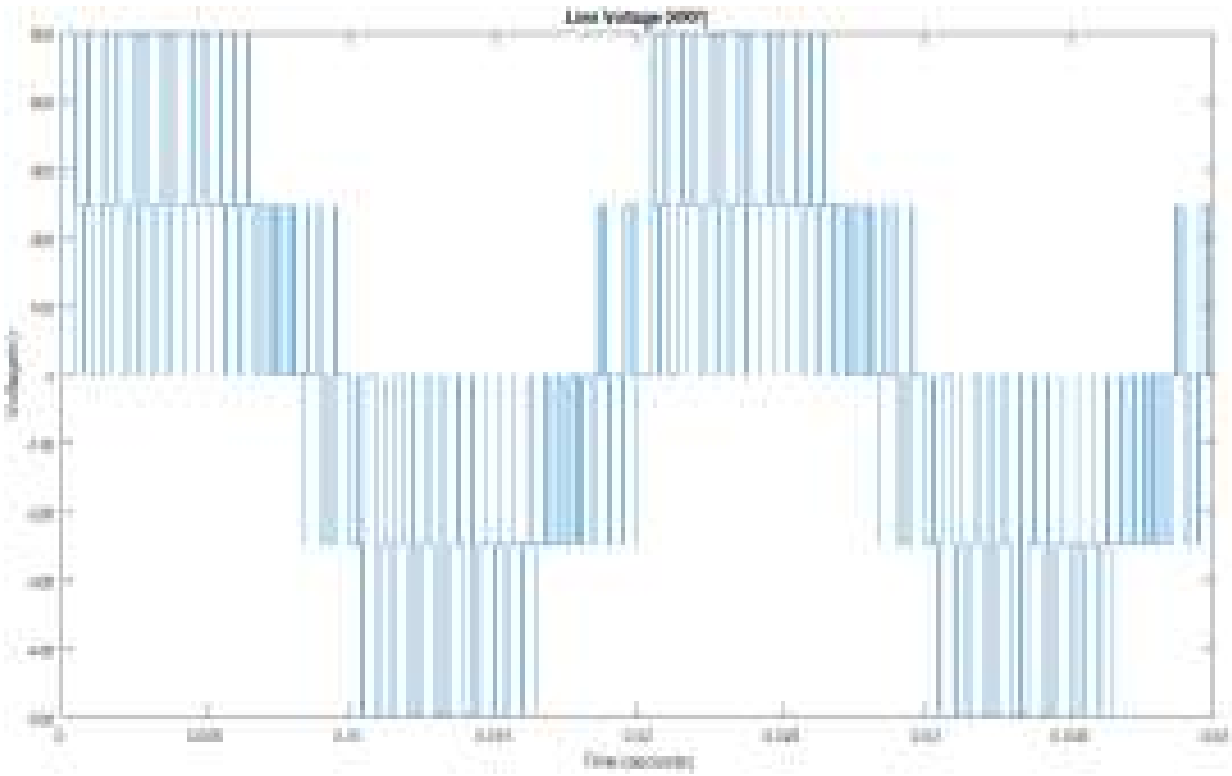

Line Voltage (V_{RY})

Result: Hence three phase three level Inverter is simulated using MATLAB/SIMULINK and its operation is studied using various waveforms.

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THREE PHASE FIVE LEVEL SINUSOIDAL PWM BASED H-BRIDGE INVERTER

Aim: To study the three phase 5-level h-bride Inverter with R-Load using MATLAB / SIMULINK software.

Circuit Diagram:

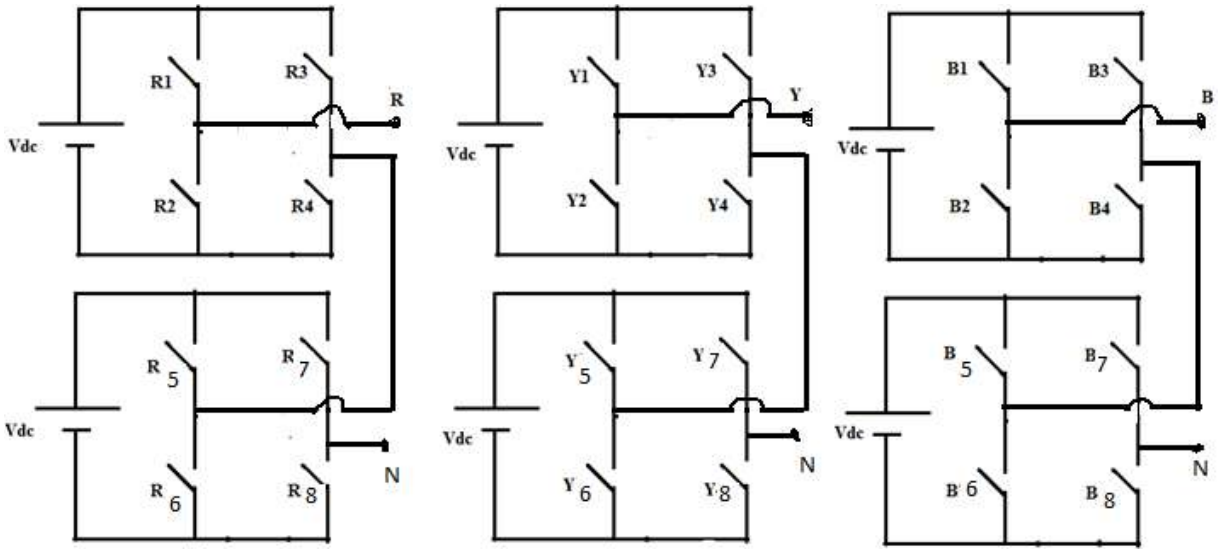

Fig.1 Three Phase Five Level Cascaded H-Bridge Inverter

Theory:

A cascaded multilevel inverter consists of a series of H-bridge (single-phase, full-bridge) inverter units. The general function of this multilevel inverter is to synthesize a desired voltage from several separate dc sources, which may be obtained from batteries, fuel cells, or solar cells. The ac terminal voltages of different level inverters are connected in series.

The output of each bridge could be summed up to generate almost sinusoidal output voltage waveform for nth level of CHMI each full bridge inverter unit forming the CHMI with separate dc. Eight semiconductors switches are able to produce five different voltage levels namely +2Vdc, +Vdc, –Vdc and -2Vdc, depending on the switching state. Each of the switching always conducts for 180 degree or half-cycle regardless of the pulse width of the quasi-square

wave so that this method will result in the equalization of the current stress in each of the components.

Each H-bridge was activated at certain amount of time at different start up angle and because each bridge was fed by separate dc source, the output of all the bridge which formed the CHMI output would be the sum of the separated dc sources for three phase nth level of CHMI inverter.

Since this topology consist of series power conversion cells, the voltage and power level may be easily scaled. The concept of this inverter is based on connecting H-bridge inverters in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each cell. The number of output voltage levels are 2n+1, where n is the number of cells. The switching angles can be chosen in such a way that the total harmonic distortion is minimized. An n level cascaded Hbridge multilevel inverter needs 2(n-1) switchingdevices where n is the number of the output voltage level.

The three phase cascaded five level inverter topology has been proposed in Fig.1. In each phase circuit consists of eight main switches in two series connected H-bridge configuration S1~S4, and S5~S8. The number of dc sources are two so the output voltage of the cascaded multilevel inverter is Vo= V1+V2. The output waveforms of multilevel inverters are in a stepped waveform therefore they have reduced harmonics compared to a square wave inverter. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge inverter. Each inverter level can generate three different voltage outputs, +2Vdc, +Vdc, –Vdc and -2Vdc, given in the table below:

Switches Turn On	**Voltage Level**
S1, S4	+Vdc
S1,S4,S5, S8	+2Vdc
S2,D4,S7,D8	0

S2,S3	-Vdc
S2,S3,S6,S7	-2Vdc

Table: the switching states of Five Level CHB

Modulation Techniques

In terms of the control strategy of a multilevel inverter, numerous researchers in the power electronic field have developed many modulation techniques. The two famous and simple modulation techniques are the Sinusoidal Pulse Width Modulation (SPWM) and, the Space Vector Pulse Width Modulation (SVPWM). A multilevel inverter switching signal can be generated using these two methods with less switching losses and harmonic distortion.

Sinusoidal Pulse Width Modulation (SPWM)

The CHMI was controlled by the SPWM where sinusoidal wave was compared with square waves to generate the switching signal that would trigger the semiconductors switches in time sequence considering the phase between the phases shift three phase inverter legs. This method used N-1 level carrier signals to generate the N-level inverter output voltage.

To generate the switching pulses of 5-level inverter utilizing sinusoidal pulse width modulation, four carrier signals were compared with one reference sine wave where the amplitude of the carrier signal was dividedinto two regions to fit the reference sine wave amplitude.

$$\text{Modulation Index (M)} = \frac{V_r}{V_c}$$

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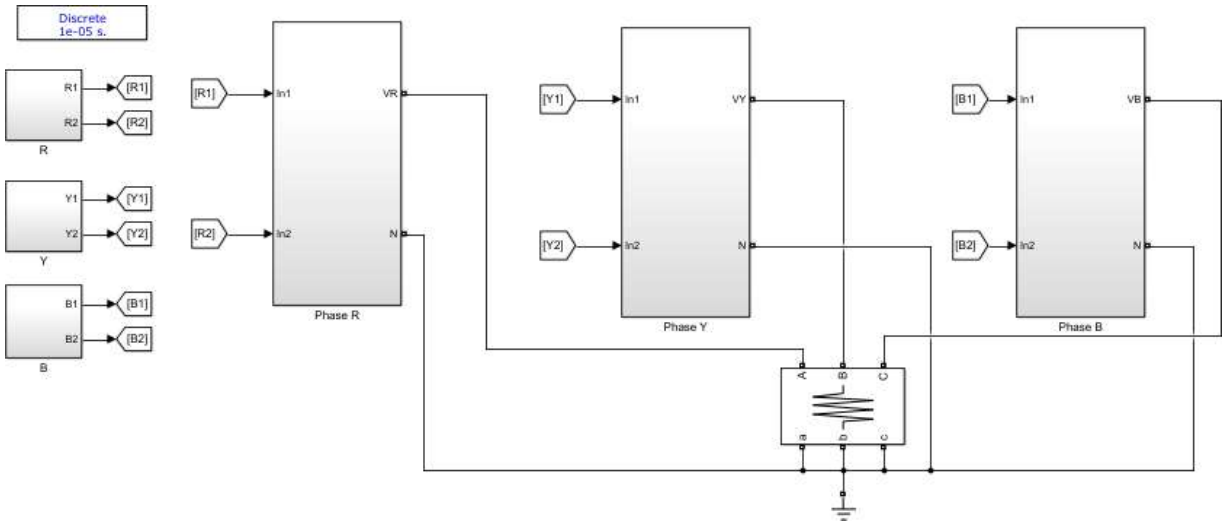
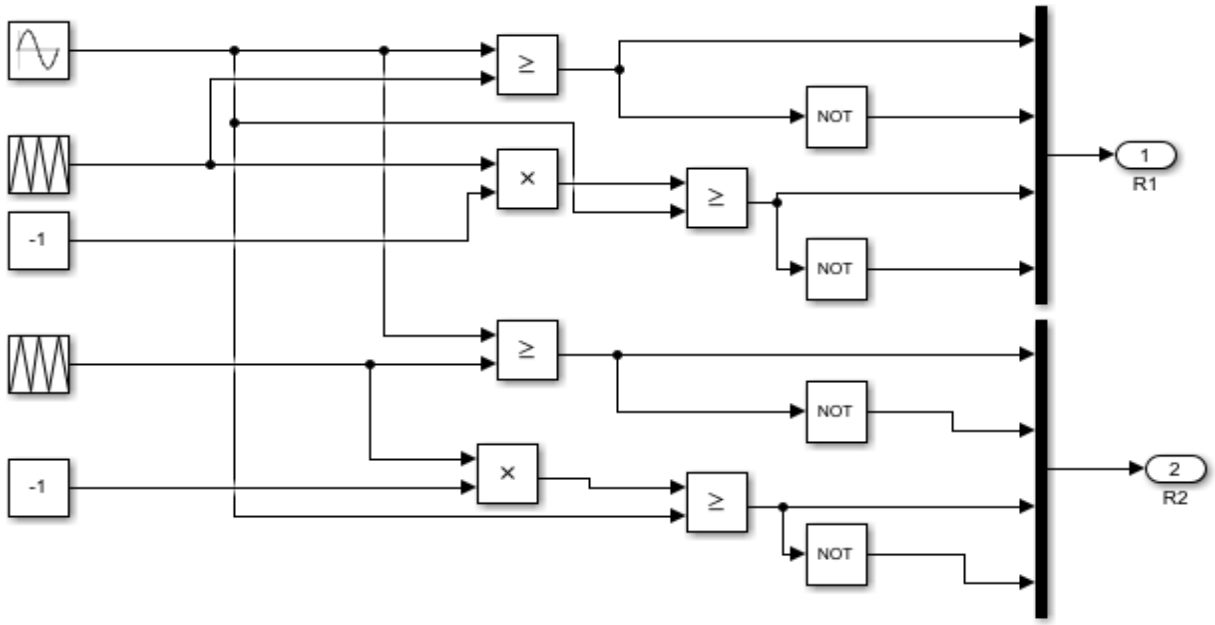
MATLAB/SIMULINK Circuit:



Three Phase Five-Level H-Bridge Inverter



3-Phase 5-Level H-bridge Sinusoidal PWM Generation for R-Phase

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Design Specifications:

Considering the Parameters for the given models followed as:

Input DC Voltage(Vdc)=250V

Supply Frequency (f) = 50 Hz,

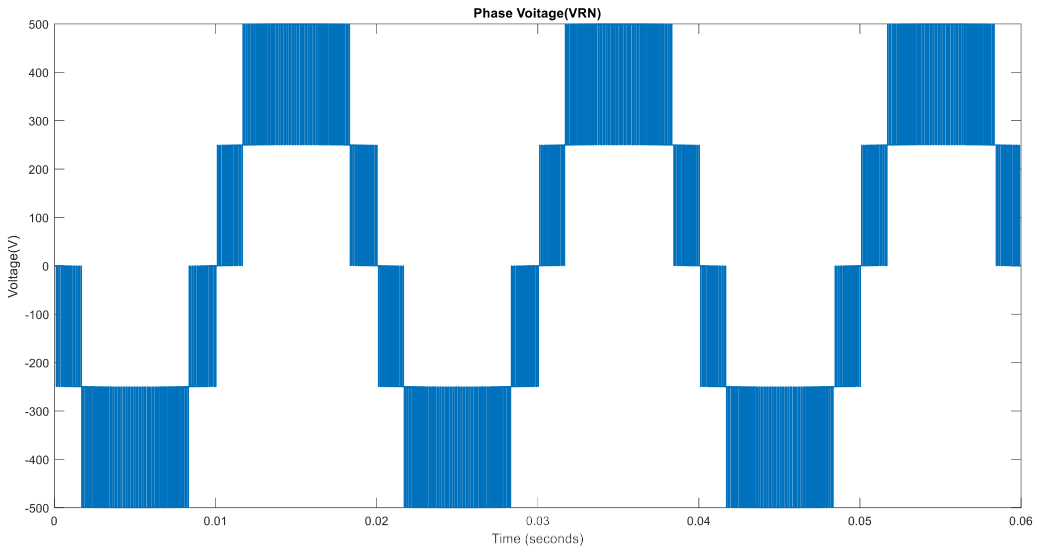
Switching Frequency = 10kHz,

Three Phase Resistive Load = 10 ohm per phase

Procedure:

1. Rig up the circuit as per the circuit diagram in MATLAB/SIMULINK Model platform.
2. Observe the output phase and line voltages.

Simulation Waveforms:



Phase Voltage (V_R)

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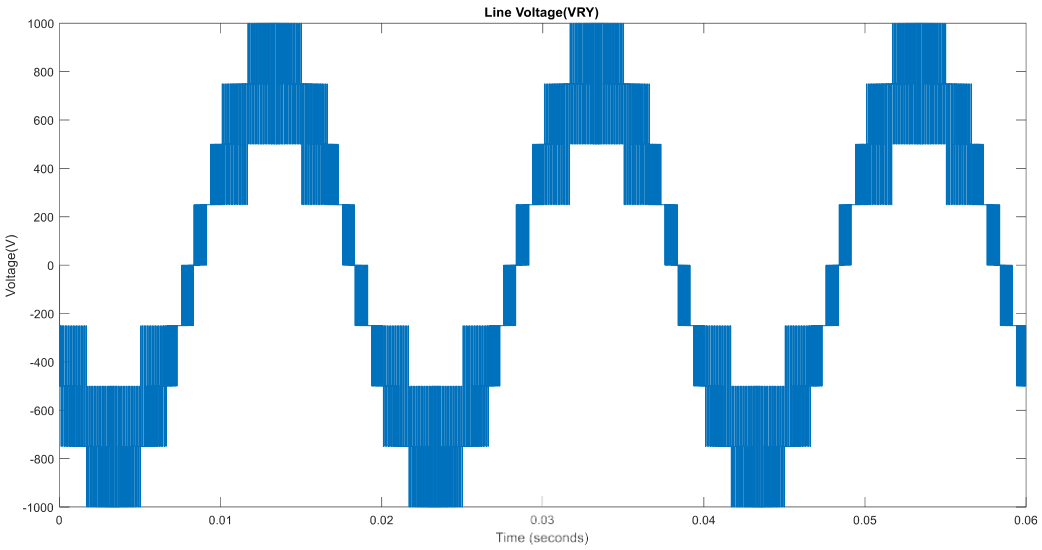

Line Voltage (V_{RY})

Result: Hencethree phase five level Inverter is simulated using MATLAB/SIMULINK and its operation is studied using various waveforms.

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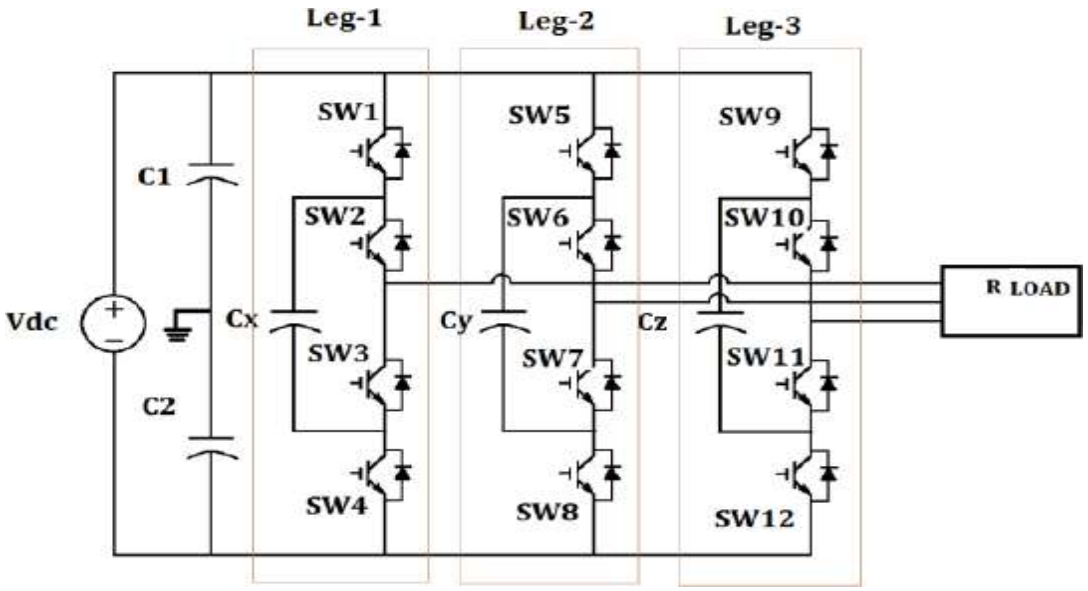
THREE PHASE THREE LEVEL SINUSOIDAL PWM BASED FLYING CAPACITOR

Aim: To study the three phase 3-level flying capacitor Inverter with R-Load using MATLAB / SIMULINK software.

Circuit Diagram:



Theory:

The three phase three level flying capacitor inverter is called so because the capacitor's floats with respect to earth potential. Flying capacitor Multi level inverter is also known as Capacitor clamped MLI.For m level flying capacitor inverter consists of 2(m-1) switches, (m-1) main capacitors and (m-1)*(m-2)/2 auxiliary capacitors are required in each phase leg. Thus a three level flying capacitor inverter consists of four switches, two main capacitors & one auxiliary capacitor in each leg.

The possible switching states are four in 3 level FCMLI. When the switches SW1, SW2 are ON and SW3, SW4 are OFF the output voltage is positive. When switches SW3, SW4 are

ON and SW1, SW2 are OFF the output voltage is negative. Zero level can be obtained in two ways that is either SW1, SW3 are ON or SW2, SW4 are ON.

Modulation Techniques

In terms of the control strategy of a multilevel inverter, numerous researchers in the power electronic field have developed many modulation techniques. The two famous and simple modulation techniques are the Sinusoidal Pulse Width Modulation (SPWM) and, the Space Vector Pulse Width Modulation (SVPWM). A multilevel inverter switching signal can be generated using these two methods with less switching losses and harmonic distortion.

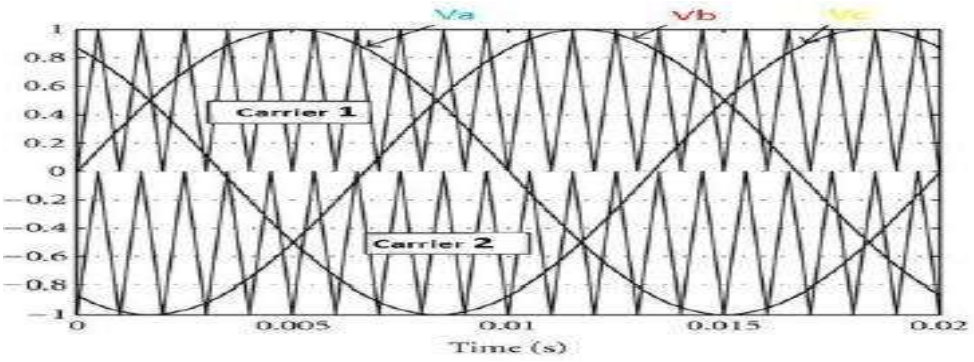
Phase disposition sinusoidal pulse width modulation:

In SPWM technique, sinusoidal reference wave is compared with triangular carrier waveform to generate pulses to switches of inverter. This traditional SPWM technique is applied to multilevel inverter by using multiple carriers. For m level inverter (m-1) carriers are required. Phase disposition SPWM has carriers in same phase above andbelow zero reference line. All the carrier signals are of same frequency and same amplitude in PD-SPWM. It is most widely used method as it provides low harmonic distortion in load voltage and current.

Phase opposition disposition sinusoidal pulse width modulation

In this POD-SPWM strategy, the carrier signals above zero reference are in same phase and carrier signals below zero reference are also in same phase, but are 180° phase shifted from those above zero.

Theoretical Waveforms:



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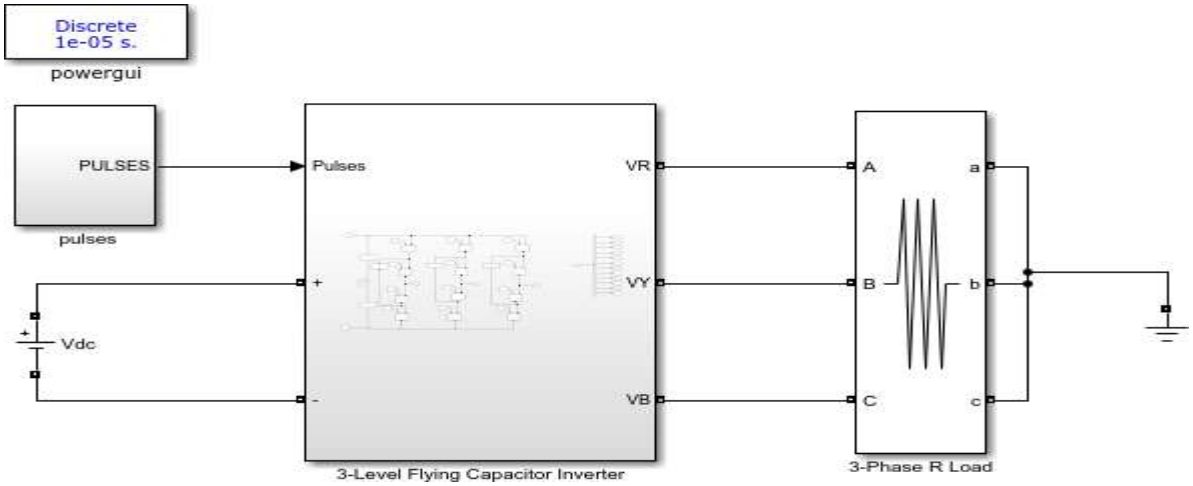
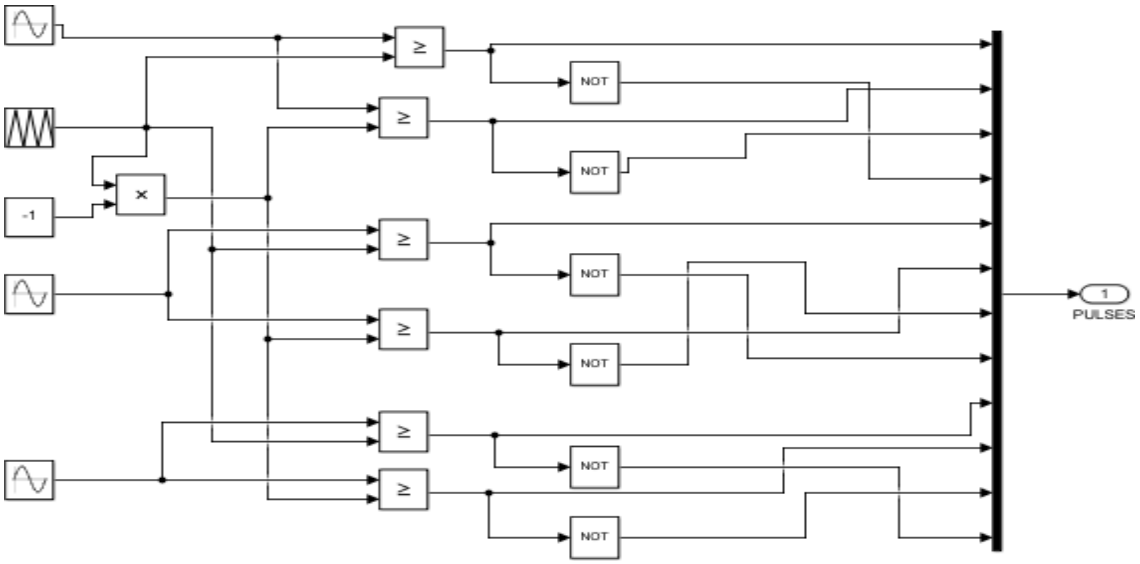
MATLAB/SIMULINK Circuit:



Three Phase Three-Level Flying Capacitor Inverter with R-Load



3-Phase 3-Level Flying Capacitor Sinusoidal PWM Generation

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Design Specifications:

Considering the Parameters for the given models followed as:

Input DC Voltage(Vdc)=250V

Capacitor with 2000μF and 1μΩ

Supply Frequency (f) = 50 Hz

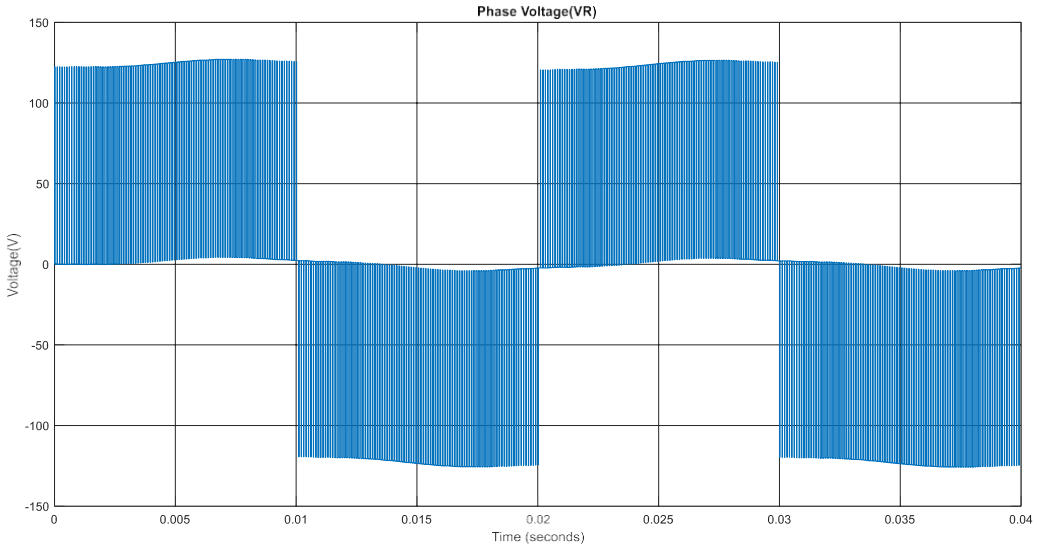
Switching Frequency = 10kHz

Three Phase Resistive Load = 10 ohm per phase

Procedure:

1. Rig up the circuit as per the circuit diagram in MATLAB/SIMULINK Model platform.
2. Observe the output phase and line voltages.

Simulation Waveforms:



Phase Voltage (V_R)

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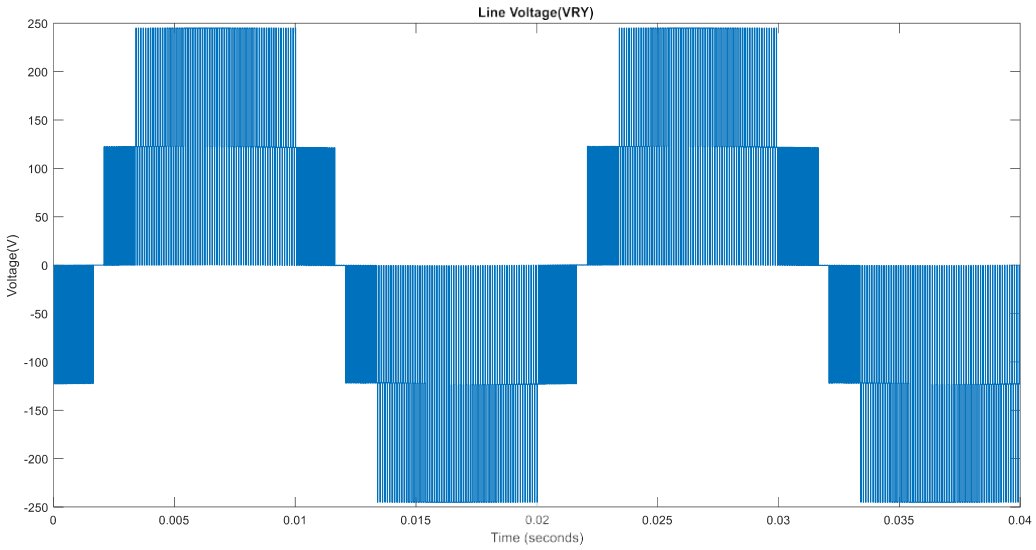

Line Voltage (V_{RY})

Result: Hence three phase three level Flying Capacitor Inverter is simulated using MATLAB/SIMULINK and its operation is studied using various waveforms.

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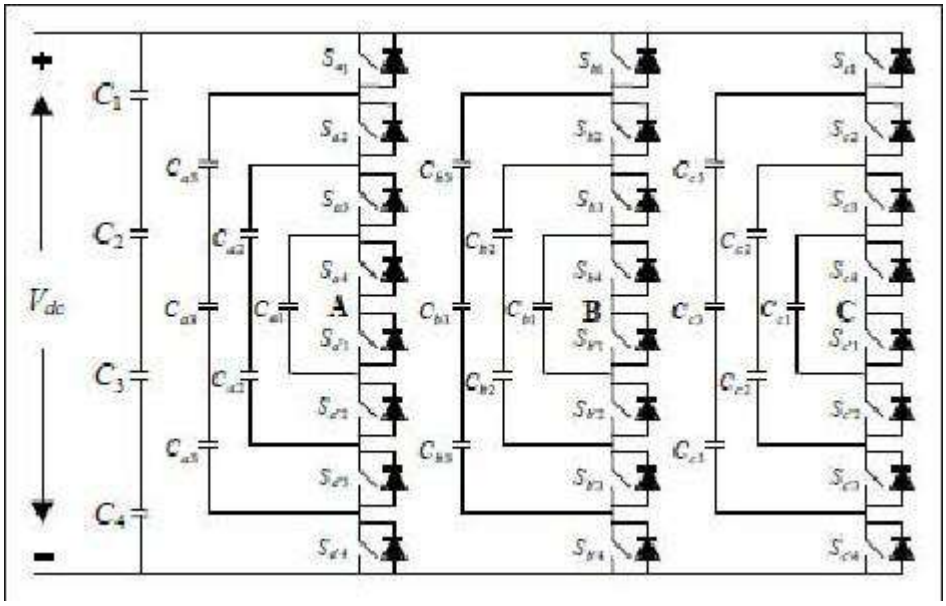
THREE PHASE FIVE LEVEL SINUSOIDAL PWM BASED FLYING CAPACITOR

Aim: To study the three phase 5-level flying capacitor Inverter with R-Load using MATLAB / SIMULINK software.

Circuit Diagram:



Theory:

The flying capacitor inverter is called so because the capacitors float with respect to earth potential. Flying capacitor Multi level inverter is also known as Capacitor clamped MLI. For m level flying capacitor inverter consists of 2(m-1) switches, (m-1) main capacitors and (m-1)*(m-2)/2 auxiliary capacitors are required in each phase leg. Thus a five level flying capacitor inverter consists of Eight switches, Four main capacitors & Six auxiliary capacitor in each leg.

The switching states of five level inverter is as follows:

For an output voltage level V0 = Vdc, all upper half switches Sa1 through Sa4 are turned ON. For an output voltage level V0 = Vdc/2, turn on three upper switches Sa1 through Sa3 and one lower switch Sa1'.For an output voltage level V0 = 0, turn on two upper switches Sa1 & Sa2 and two lower switch Sa1' & Sa2'.For an output voltage level V0 = -Vdc/2, turn on one upper switch

Sa1 and three lower switches Sa1' through Sa3'. For an output voltage level V0 = -Vdc, turn on all lower half switches Sa1' through Sa4'**.**

Table 1 shows the voltage levels and their corresponding switch states. State condition 1 means the switch is ON, and state 0 means the switch is OFF.

V_0	Sa_1	Sa_2	Sa_3	Sa_4	Sa_1'	Sa_2'	Sa_3'	Sa_4'
Vdc	1	1	1	1	0	0	0	0
Vdc/2	1	1	1	0	1	0	0	0
0	1	1	0	0	1	1	0	0
-Vdc/2	1	0	0	0	1	1	1	0
-Vdc	1	0	0	0	1	1	1	1

Modulation Techniques

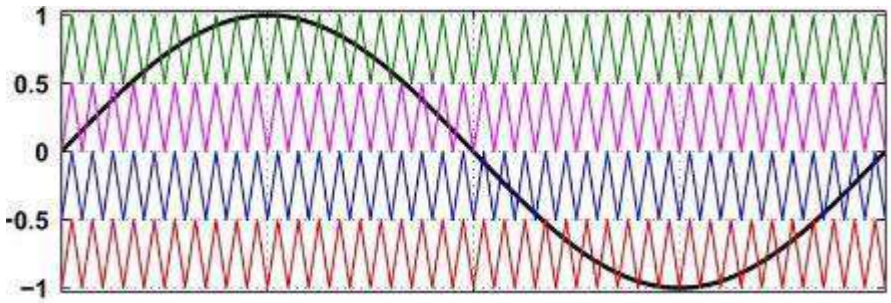
In terms of the control strategy of a multilevel inverter, numerous researchers in the power electronic field have developed many modulation techniques. The two famous and simple modulation techniques are the Sinusoidal Pulse Width Modulation (SPWM) and the Space Vector Pulse Width Modulation (SVPWM). A multilevel inverter switching signal can be generated using these two methods with less switching losses and harmonic distortion.

Phase disposition sinusoidal pulse width modulation:

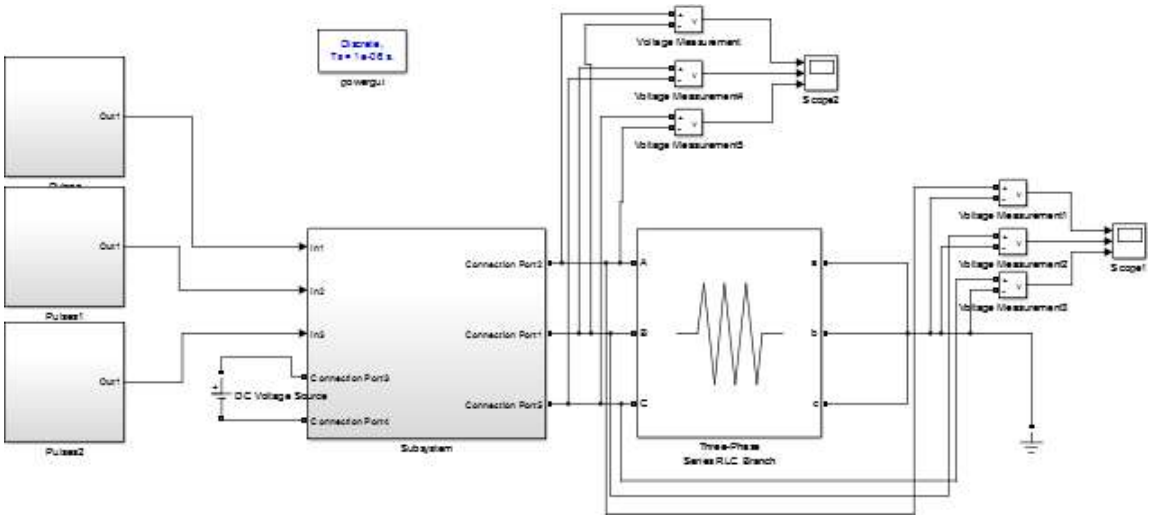
In SPWM technique, sinusoidal reference wave is compared with triangular carrier waveform to generate pulses for applying to the switches of inverter. This traditional SPWM technique is applied to multilevel inverter by using multiple carriers. For m level inverter (m-1) carriers are required. Therefore, for five level inverter, sinusoidal reference wave is compared with four carrier waveforms. Phase disposition SPWM has carriers in same phase above and below zero

reference line. All the carrier signals are of same frequency and same amplitude in PD-SPWM. It is most widely used method as it provides low harmonic distortion in load voltage and current.

Theoretical Waveforms:



MATLAB/SIMULINK Circuit:



Three Phase Five Level Flying Capacitor Inverter with R-Load

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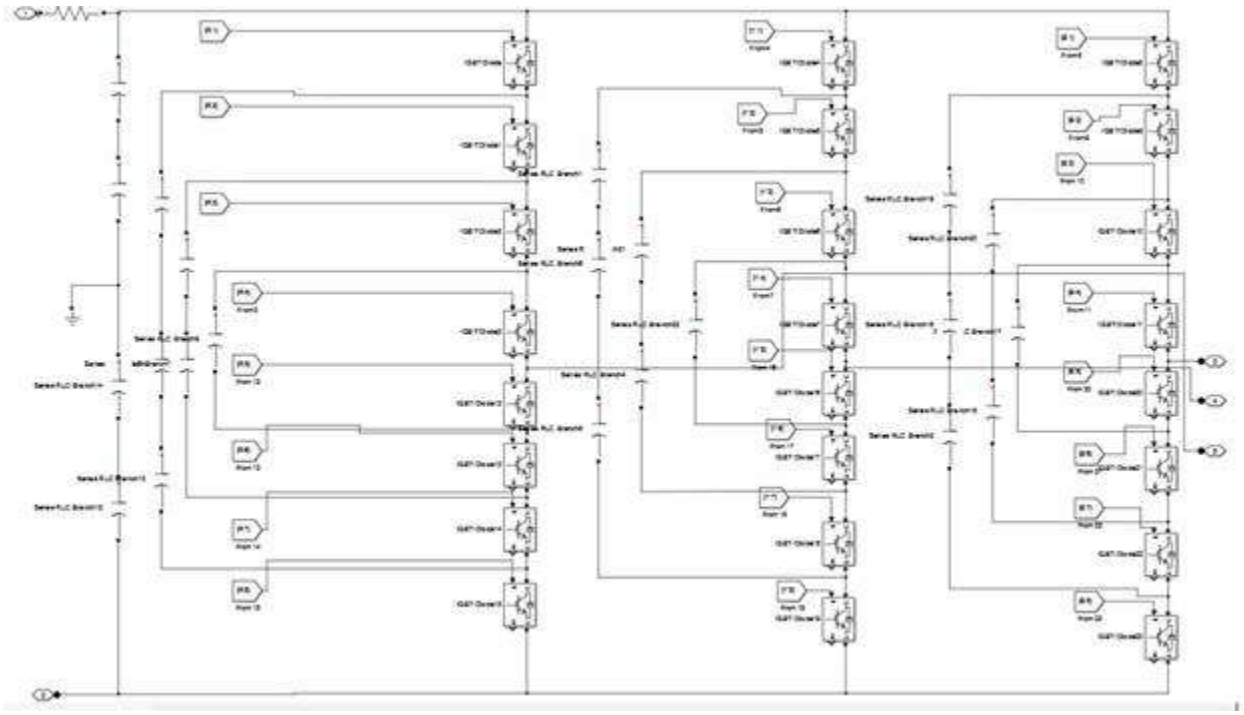
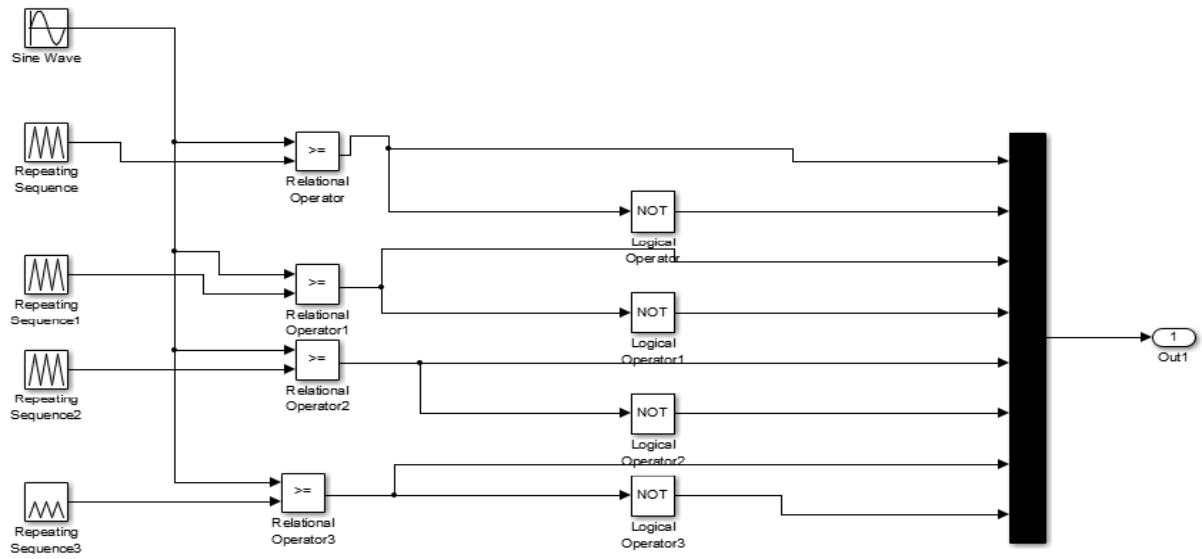


Simulink Model of Five level Flying Capacitor Inverter



Inverter Pulse Generation (Sinusoidal PWM)

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Design Specifications:

Considering the Parameters for the given models followed as:

Input DC Voltage(Vdc)=400V

Capacitor with 40000µF

Supply Frequency (f) = 50 Hz

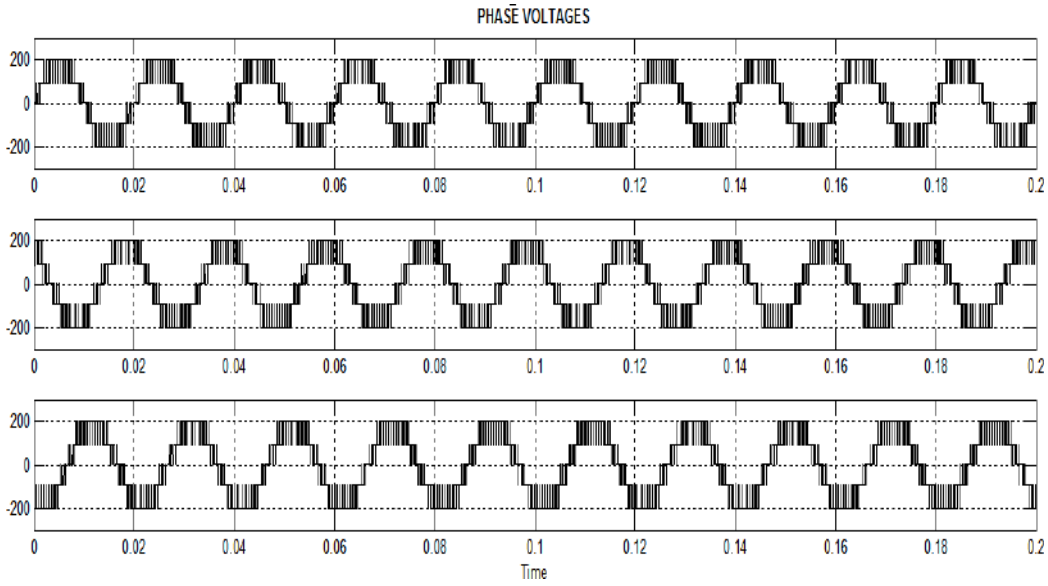
Switching Frequency = 1kHz

Three Phase Resistive Load = 50 ohm per phase

Procedure:

1. Rig up the circuit as per the circuit diagram in MATLAB/SIMULINK Model platform.
2. Simulate the circuit for the phase and line output voltages.

Simulation Waveforms:



Phase Voltage

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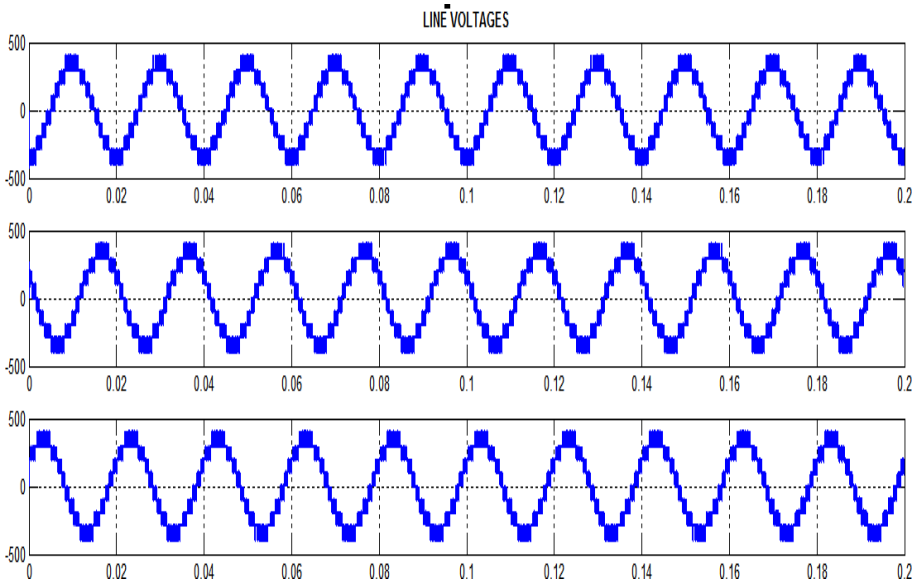

Line Voltage (V_{RY})

Result: Three phase Five Level Flying Capacitor Inverter is simulated using MATLAB/SIMULINK and its operation is studied using various waveforms.

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SPACE VECTOR PULSE WIDTH MODULATION TECHNIQUE FOR SINGLE PHASE INVERTER

Aim: Simulation of single phase inverter with Space Vector PWM Technique.

Circuit Diagram:

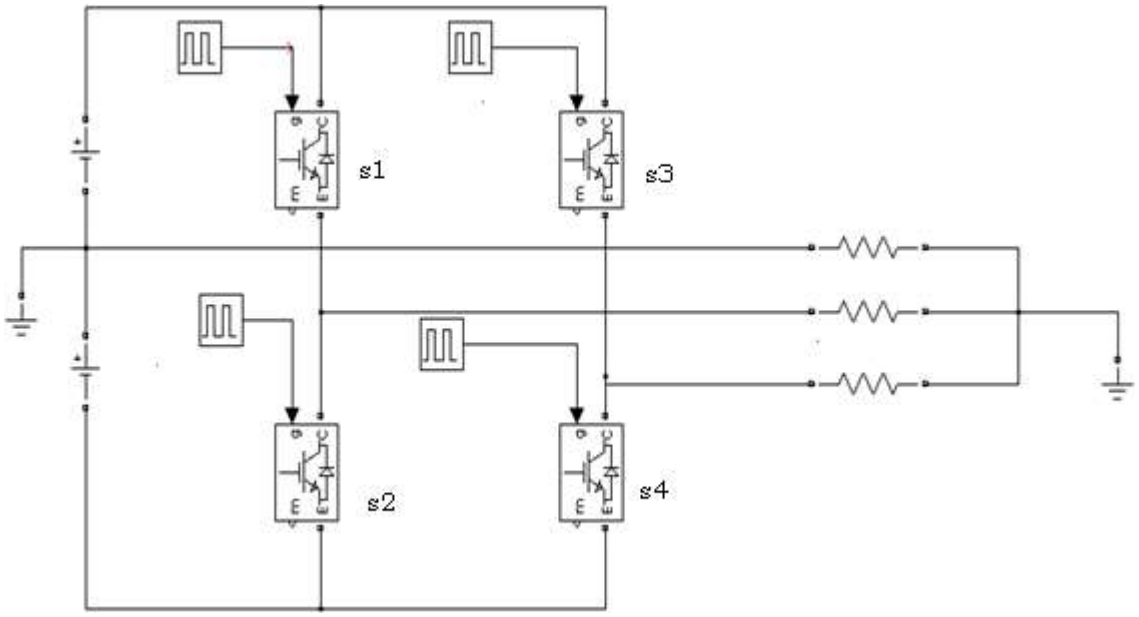

Fig.1. Circuit Diagram of single phase inverter

Theory of operation :

Principle of Space Vector PWM :

- Treats the sinusoidal voltage as a constant amplitude vector Rotating at constant frequency
- This pwm technique approximates the reference voltage Vref by a combination of the four switching patterns V1 to V4.
- The coordinate transformation from abc to dq frame is carried out where three phase voltage vector is transformed into a vector in the stationary d-q coordinate frame which represents the spatial vector sum of the three phase voltages.

- The vectors V1 to V4 devide the plane into four sectors , each sector of 90^0
- Vref is generated by two adjacent non- zero vectors and two zero vectors.

Realization of Space Vector PWM

Step 1 : Determine Vd, Vq, Vref and angle 'α'

Step 2 : Determine time duration T1, T2, T0

Step 3 : Determine the switching time of each switch (S1 to S4)

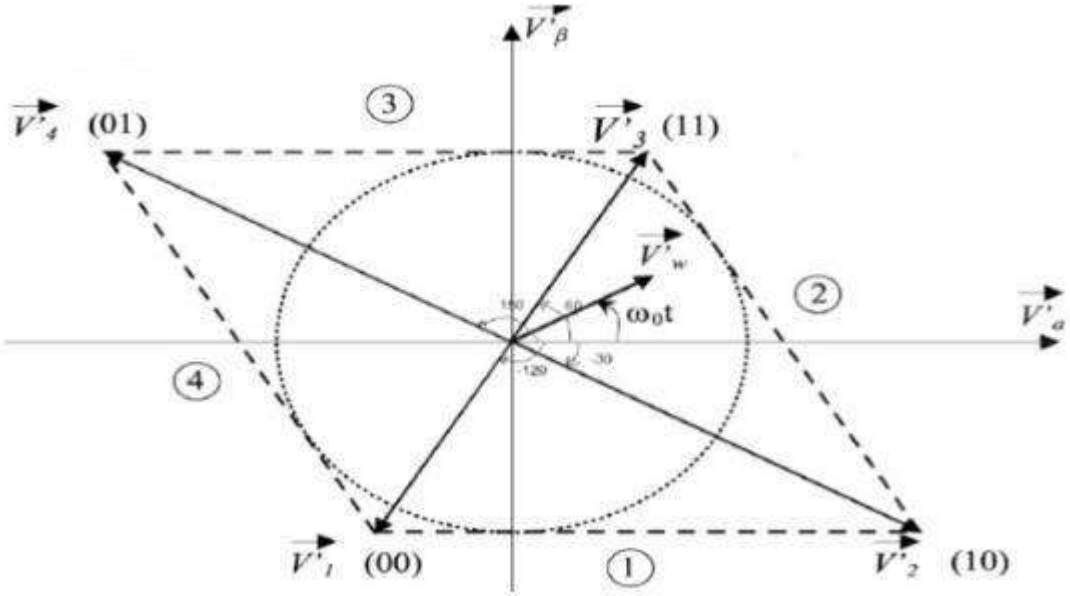

Fig.2 Space vector representation

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Table 1: Three phase voltage representation

			Phase voltage			line voltages		
	Sa	Sb	Van	Vbn	Vcn	Vab	Vbc	Vca
V1	0	0	-Vdc/3	-Vdc/3	-2Vdc/3	0	-Vdc	Vdc
V2	1	0	Vdc	-Vdc	0	2Vdc	-Vdc	-Vdc
V3	1	1	Vdc/3	Vdc/3	-2Vdc/3	0	Vdc	-Vdc
V4	0	1	-Vdc	Vdc	0	-2Vdc	Vdc	Vdc

Table 2:Two phase voltage representation

	Sa	Sb	Vd	Vq	V=Vd+jVq
V1	0	0	-Vdc/3	-Vdc/√3	(2Vdc/3)e^-j2Π/3
V2	1	0	Vdc	-Vdc/√3	(2Vdc/√3)e^-jΠ/6
V3	1	1	Vdc/3	Vdc/√3	(2Vdc/3)e^jΠ/3
V4	0	1	-Vdc	Vdc/√3	(2Vdc/√3)e^j5Π/6

Switching time duration for sector 1:

$V_{\alpha}' \rightarrow$

$V_1 T_1 *COS(-120^0) + V_2 T_2 *COS(-30^0) = V_S * T_S *COS(180^0 +60^0 +\theta)$

$V_1 T_1 *(-1/2) + V_2 T_2 *COS(\sqrt{3}/2) = - V_S * T_S *COS(60^0 +\theta)$

$V_{\beta}' \rightarrow$

$V_1 T_1 *COS(210^0) + V_2 T_2 *COS(120^0) = V_S * T_S *COS(180^0 +30^0 -\theta)$

$V_1 T_1 *(-\sqrt{3}/2) + V_2 T_2 *COS(-1/2) = - V_S * T_S *COS(30^0 -\theta)$

$T_1 = (V_S *T_S * COS\theta)/ V_1$

$T_2 = (V_S * T_S * SIN\theta)/ V_2$

Switching time duration for any sector

$$T_1 = \frac{Vs\,Ts}{V1} \text{ COS } (\theta+(\frac{n-1}{2})\,\pi\,)$$

$$T_1 = \frac{Vs\,Ts}{V2} \text{ sin } (\theta-(\frac{n-1}{2})\,\pi\,)$$

$T_0 = T_S – (T_1 + T_2)$

T_S is the sampling time.

Table 3: Switching times of each sector

SECTOR 1	SECTOR 2
$T_1 = \frac{3\,V_{ref}Ts\cos(\alpha)}{2V_{dc}}$ $T_2 = \frac{\sqrt{3}\,V_{ref}Ts\sin\alpha}{2V_{dc}}$ $T_0 = Ts-(T_1+T_2)$	$T_2 = \frac{-\sqrt{3}\,V_{ref}Ts\sin(\alpha)}{2V_{dc}}$ $T_3 = \frac{-3\,V_{ref}Ts\cos(\alpha)}{2V_{dc}}$ $T_0 = Ts-(T_2+T_3)$
SECTOR 3	**SECTOR 4**
$T_3 = \frac{-3\,V_{ref}Ts\cos(\alpha)}{2V_{dc}}$ $T_4 = \frac{-\sqrt{3}\,V_{ref}Ts\sin(\alpha)}{2V_{dc}}$ $T_0 = Ts-(T_3+T_4)$	$T_4 = \frac{\sqrt{3}\,V_{ref}Ts\sin(\alpha)}{2V_{dc}}$ $T_5 = \frac{3\,V_{ref}Ts\cos(\alpha)}{2V_{dc}}$ $T_0 = Ts-(T_4+T_5)$

Table 4 : Switching time of each transistor

sector	Upper switches	Lower switches
1	S1=T2+To/2 S3=To/2	S2=T1+To/2 S4=T1+T2+To/2
2	S1=T1+T2+To/2 S3=T2+To/2	S2= To/2 S4=T1+To/2
3	S1=T1+T2+To/2 S3=T1+To/2	S2=T2+To/2 S4= To/2
4	S1= To/2 S3=T1+To/2	S2=T1+T2+To/2 S4=T2+To/2

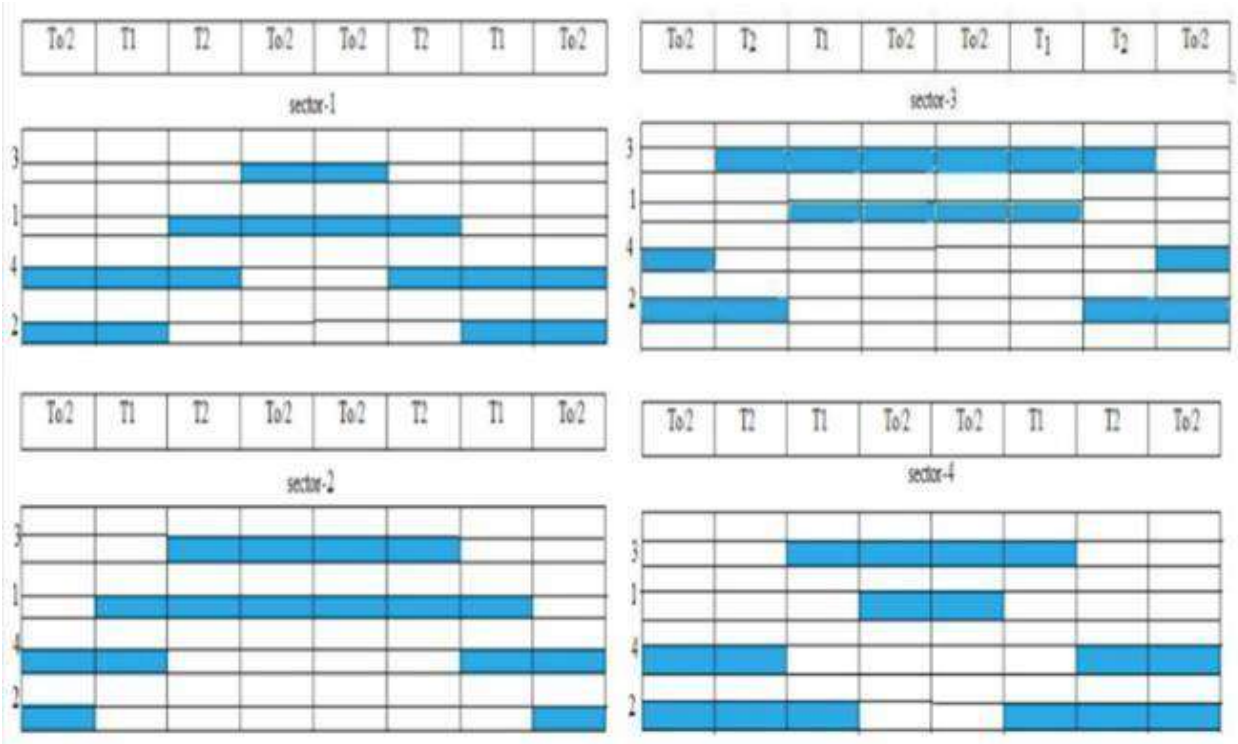

Fig. 3 Switching times of each sector

Table 4 : Magnitude, angle and sector representation

Vectors	Magnitude	Angle (α)
V_1	$2/3\ V_{dc}$	-120^0
V_2	$2/\sqrt{3}\ V_{dc}$	-30^0
V_3	$2/3\ V_{dc}$	60^0
V_4	$2/\sqrt{3}\ V_{dc}$	150^0

Sector	Range of angles
1	$-120^0 < \alpha < -30^0$
2	$-30^0 < \alpha < 60^0$
3	$60^0 < \alpha < 150^0$
4	$150^0 < \alpha < 180^0$
4	$-180 < \alpha < -120^0$

At any instant, the combination of the upper/lower switch signals will give an 'M' shaped wave, which is compared with a triangular signal to give gate pulses to the switches in the converter.

Procedure:

1. Rig up the circuit as per the diagram.
2. Follow the steps for realization of Space Vector Modulation.
3. The modulating wave (M shaped wave) must be compared with carrier wave (triangular wave) and linear modulation is considered.
4. For linear modulation M.I is less than 1 and hence the reference magnitude is considered to be less than carrier wave magnitude.
5. The carrier wave frequency is considered as 1000Hz.
6. Run the simulation and save the waveforms in workspace.

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Simulation Circuits:

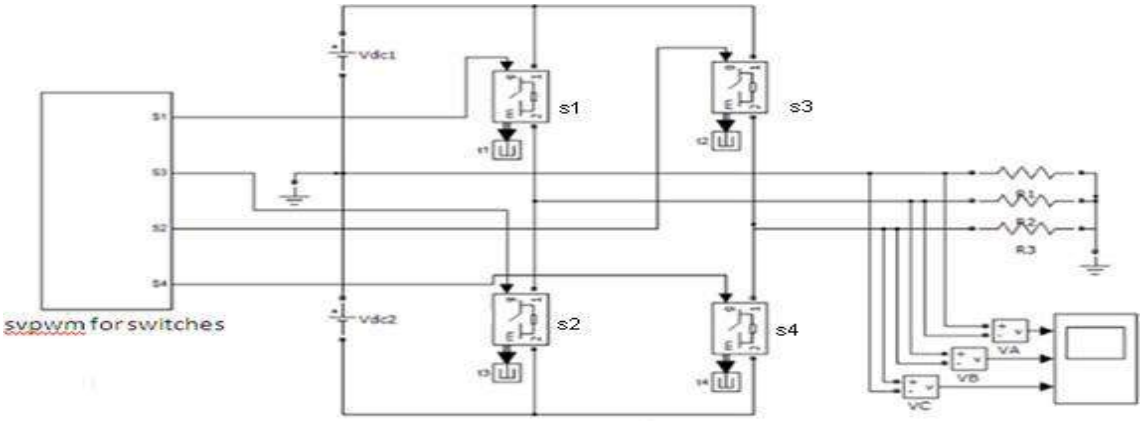

Fig.4 Single phase inverter with SVPWM

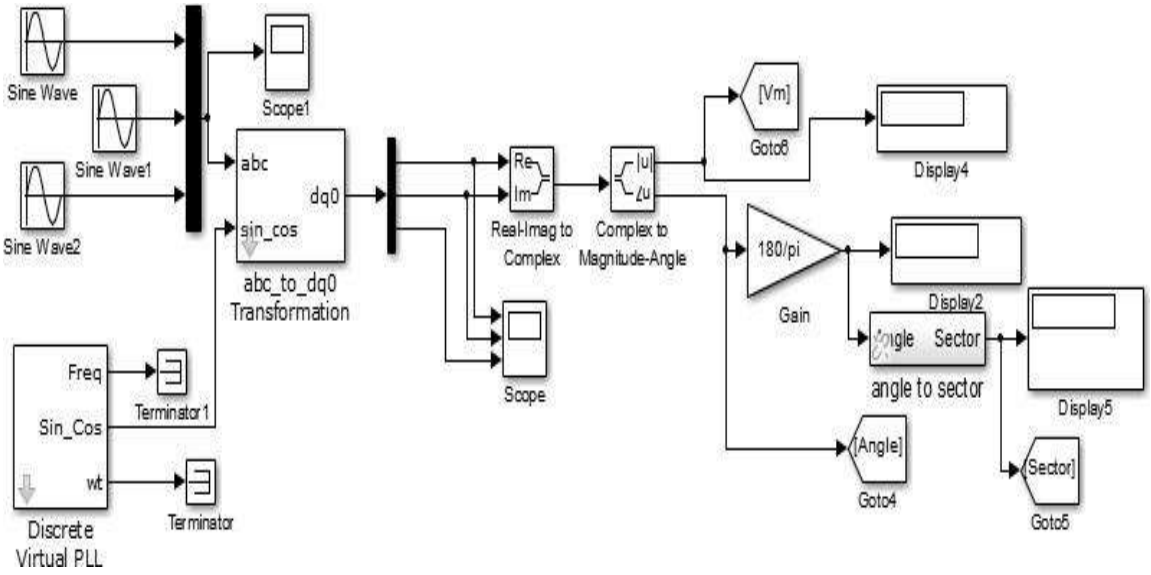

Fig.5 Angle & sector determination

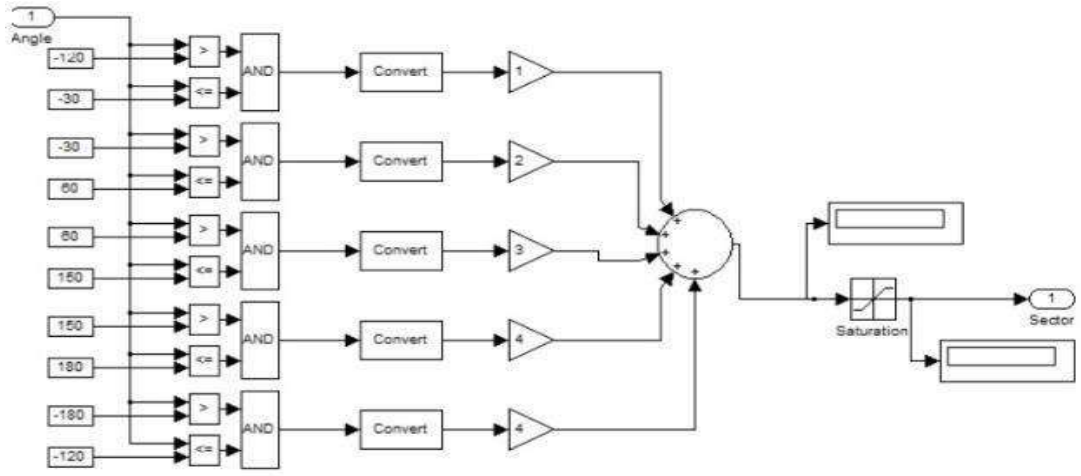

Fig.6 Angle to sector conversion

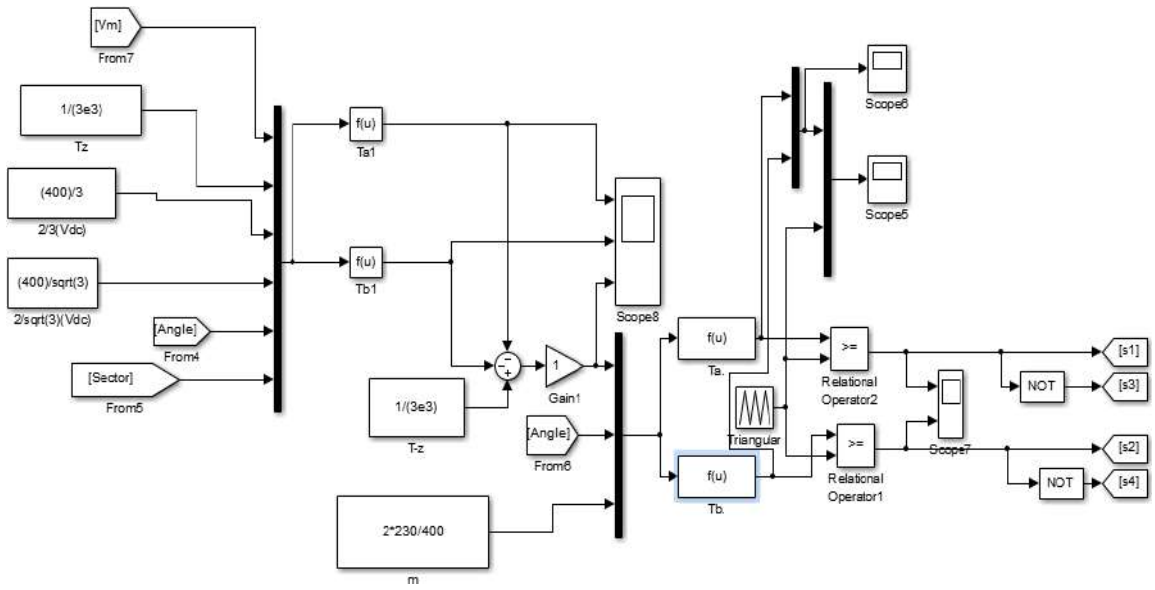

Fig.7 Pulse Generation

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Ta1 = (u[6]==1)*(u[1]*u[2]*(cos(u[5]))/u[3])+(u[6]==2)*(-u[1]*u[2]*(sin(u[5]))/u[4])+(u[6]==3)*
(-u[1]*u[2]*(cos(u[5]))/u[3])+(u[6]==4)*(u[1]*u[2]*(sin(u[5]))/u[4])

Tb1 = (u[6]==1)*(u[1]*u[2]*(sin(u[5]))/u[4])+(u[6]==2)*(-u[1]*u[2]*(cos(u[5]))/u[3])+(u[6]==3)*
(-u[1]*u[2]*(sin(u[5]))/u[4])+(u[6]==4)*(u[1]*u[2]*(cos(u[5]))/u[3])

Ta = sqrt(3)*u[3]*sin(u[2]-pi/3)

Tb = sqrt(3)*u[3]*sin(u[2]-2*pi/3)

Fs = 10000 Hz

Simulation Results:

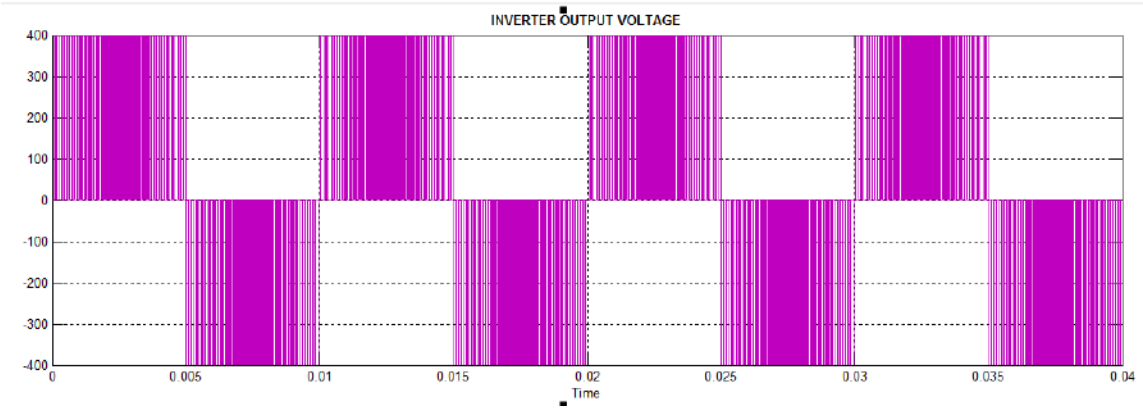

Fig.8 Inverter output voltage

Result : The Single phase two leg inverter is simulated using MATLAB/ SIMULINK and its operation is studied using various waveforms.

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GENERATION OF SQUARE WAVEFORM USING FPGA XILINX

Aim : To generate square waveform using FPGA Xilinx and MATLAB/Simulink.
Software requirements and version : MATLAB/Simulink 2013a, Xilinx 2013
Simulink Model:

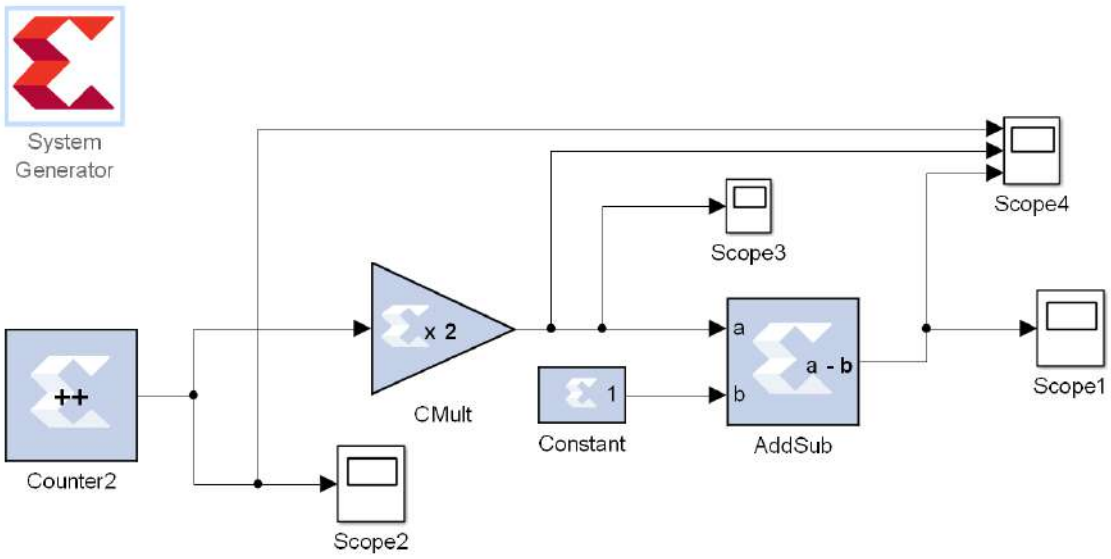

Fig.1 Simulink model for Square wave generation

Procedure:

1. Build the simulink model as shown in Fig.1.
2. Open MATLAB simulink library & add system generator from Xilinx Blockset libraries: Basic Elements, Tools, and Index to the new model. Enter the specifications of the system generator as per the following Fig.2.
3. Add CMult block from Xilinx Blockset libraries: Math, Floating-Point. Enter the specifications of CMult block as per the following Fig.3.
4. Add constant block from Xilinx Blockset libraries: Basic Elements, Control Logic, Math, Floating-Point and Index. Enter the specifications of constant block as per the following Fig.4.
5. Add Addsub block from Xilinx Blockset libraries: Math, Floating-Point and Index. Enter the specifications of Addsub block as per the following Fig.5.
6. Add counter block from Xilinx Blockset libraries: Basic Elements, Control Logic, Math, and Index. Enter the specifications of counter block as per the following Fig.6.
7. Add scope to view the outputs and run the simulation.

Fig.2 System Generator Specifications

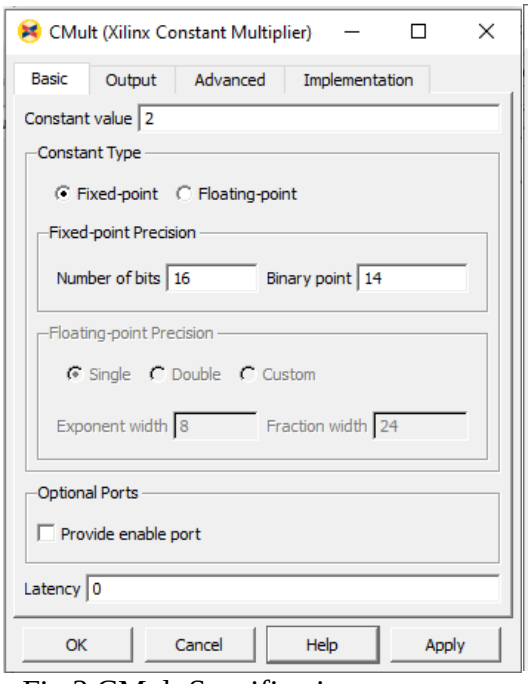

Fig.3 CMult Specifications

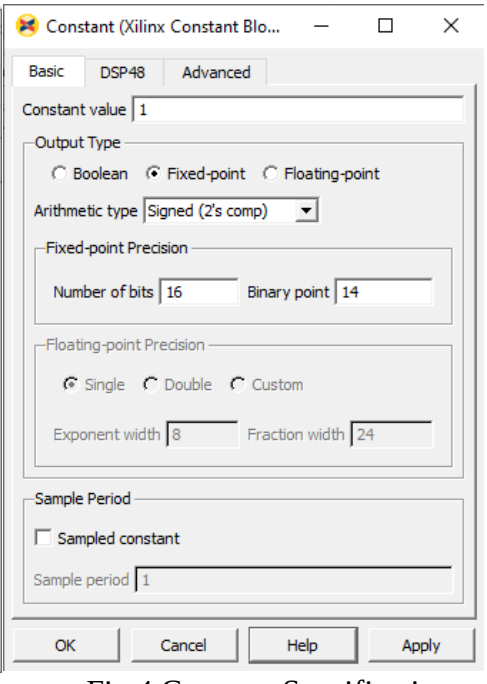

Fig.4 Constant Specifications

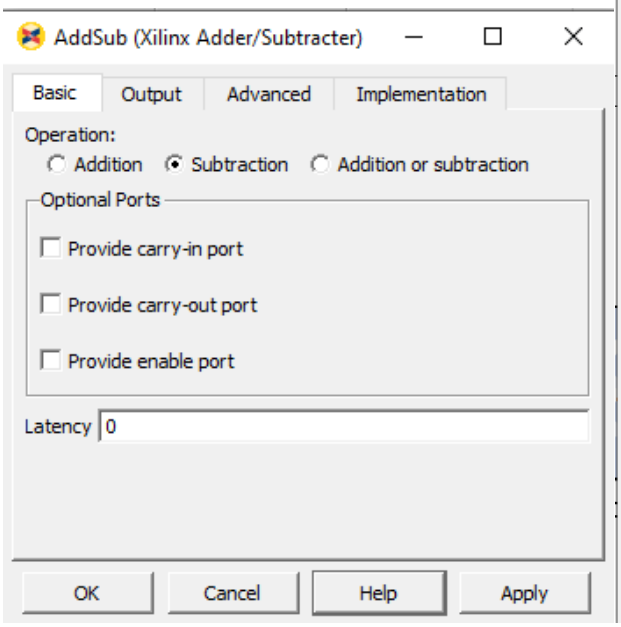

Fig.5 Add sub Specifications

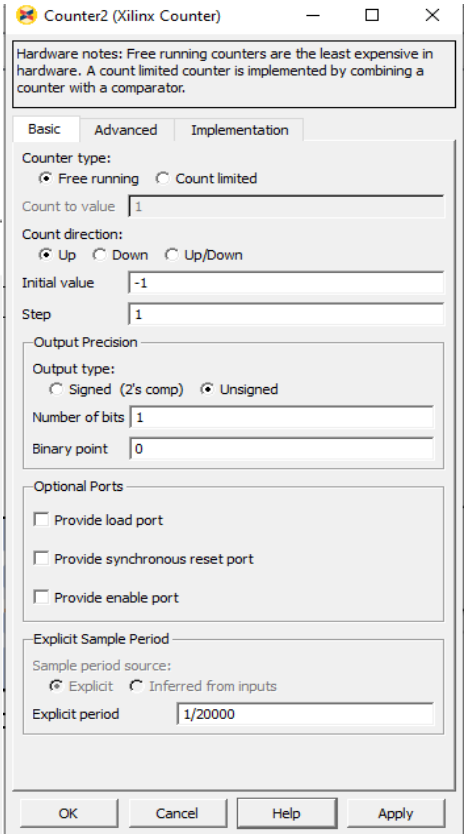

Fig.6 Counter Specifications

Output waveform:

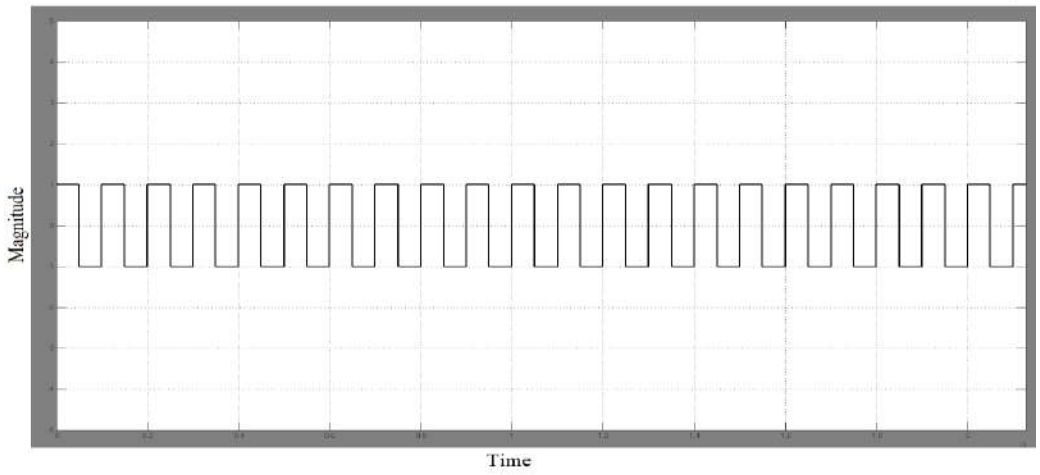

Fig.7 Output waveform

Result:

Square waveform using FPGA –Xilinx is generated and studied.

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