G. Narayanamma Institute of Technology and Science (For Women)
(AUTONOMOUS)

Department of ECE

VLSI Design Lab

VLSI Design Lab :

The VLSI Design lab is established in the year 2001 in the Department of Electronics and Communication Engineering. It contains well-established hardware and software according to the Curriculum in the field of VLSI Design. It is equipped with sufficient number of systems with online UPS and networking.

The VLSI Design lab is a dynamic and essential space for innovation in integrated circuit design. The lab provides students with hands-on experience in designing, implementing, and testing integrated circuits. It helps them understand the practical aspects of VLSI design, from basic concepts to complex chip architectures. The lab is often used for cutting-edge research in semiconductor technology. Researchers explore new design methodologies, circuit architectures, and fabrication techniques.

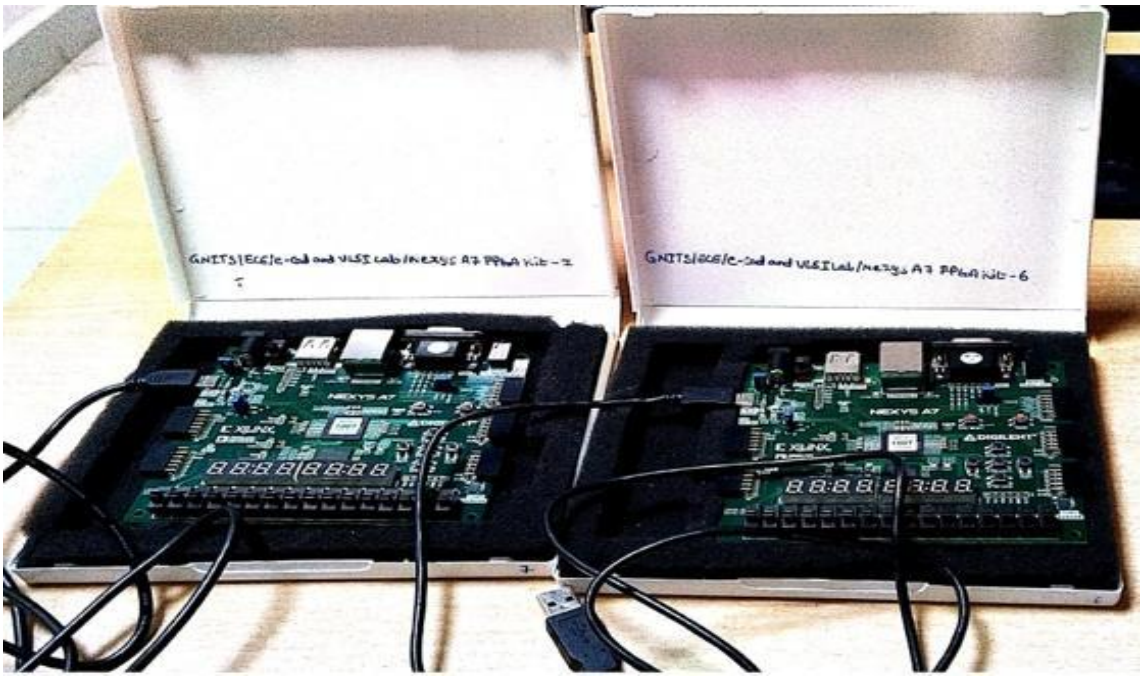
The VLSI Design lab is often utilized for student projects that involve the design, simulation, and implementation of integrated circuits. These projects allow students to apply theoretical knowledge to practical problems

Faculty associated with VLSI Design Lab:

S.No	Name of the faculty	Designation	Area of Research
1	Dr. K. Ragini,	Professor	Low Power VLSI Design
2	Mr.G. Krishna Kishore	Assistant Professor	VLSI Design
3	Mr. V. Radha Krishna	Assistant Professor	VLSI Design
4	Mr. B. Sreekanth Reddy	Assistant Professor	VLSI Design & Internet Of Things
5	Mr.V.Shankar	Assistant Professor	Low Power VLSI Design and Analog &Mixed signal Design.
6	Mrs.P.Roopa Ranjani	Assistant Professor	Implantable Medical Devices
7	Mrs.M.Shanthi	Assistant Professor	Internet Of Things

Photos:

VLSI Design Lab



Nexys 4 A7 FPGA boards

Facilities

VLSI Design lab has two laboratories with the following software's and hardware kits. The facilities are available for all faculty and students who would like to participate in VLSI R&D activities.

Softwares:

1. Xilinx Vivado System Edition 2018.1
2. Xilinx ISE 13.4 Version Edition
3. Mentor Graphics Back End Tools-HEP-1
4. Mentor Graphics Front End Tools-HEP-2

Hardware Kits:

S.No	Name	Quantity
1	Nexys 4 A7 FPGA boards	7
2	Spartan 6E boards	7
3	Electronic explores kit	5

Funded research projects carried out in VLSI Design lab

S.No	Title of the Project	Funding Agency	Sanctioned Amount in Lakhs	Faculty Associated
1	Third EYE, Automatic hand Sanitizer, Lora Smart city & Design of High Performance Approximate Redundant Binary Multiplier using 4:2,5:2,7:2 Compressors	SEED	2.59L	Dr. K.Ragini
2.	Embedded Systems in Internet of Things (STTP)	AICTE	3.69L	Dr. K.Ragini
3	Smart Kitchen Management System	SEED	0.36 L	Mr.B Sreekanth Reddy

Faculty as Resource Persons

S.No.	Name of the Program	Lecture Topic	Name of the Faculty	Duration	Venue	Organized by
1	Guest Lecture	Functional Approach to VLSI Design	B.Sreekanth Reddy	Assistant Professor	GNITS	GNITS
2	Guest Lecture	Introduction to VLSI	B.Sreekanth Reddy	Assistant Professor	Sridevi Women's Engineering College	Sridevi Women's Engineering College

Faculty Awards and Recognitions

S.No.	Name of the Faculty	Designation	Details of the award and recognition
1	Dr. K. Ragini	Professor	Best paper award, ICMACC,30-12-2022
			NPTEL Certification of appreciation award, Jan-Dec 2020.
2	V. Radha Krishna	Assistant Professor	NPTEL Discipline Star,SWAYAM NPTEL, JAN-APR 2023

Details of Faculty Professional Body Memberships

S. No	Faculty Name	MembershipNo.						
		IEEE	ISTE	IETE	ISOI	IEI	Internet Society	OTHERS
1	Dr. K. Ragini			M 216334		F-122073-6		
2	Mr. V. Radha Krishna			M-181404				
3	M Shanthi			F-503999				

Industry interactions

List of MOUs with VLSI industries

S.No.	Name of the industry	Impact
1.	Maven Silicon Softech Private Limited, Bangalore, India	Training in the field of VLSI Design Providing Internships to the students in VLSI Design

List of Industry persons associated

Guest lecturers delivered by Industry experts during last 3 Years

S.No	Resource Person Name	Industryassociated	Title	Date
1.	CH.Venkata Prthyusha	MoS Chip Semiconductors	Current trends in verifying complex chips	19/08/2023
2.	Mr .K.A.Vinnalan	Application Engineer, Corel technologies,	Tanner Design Flow using Mentor Graphics tools	31/08/2022

Internships Opportunities in VLSI related industries

S.No	Name of the Industry	Name of the Student&RollNo
1	Silicon Labs	20251A0477, MEKA TANUSHA
2	Medha Servo Drives Pvt.ltd	20255A0403,T.Pavani
3.	Channel Soft IT Services Pvt. LTd	18251A0403, K Sri Charita
4.	M/s Valuelabs, Hyd	16251A0494 M.Varunitha

Academic projects carried out by Student Projects

BTECH 2023-24 (20-24 BATCH)

	Roll No.	Title of the Project	Name of the Supervisor
B4	20251A0496	Design of Data Encoding Technique for Reducing Energy Consumption in Network-on-Chip (NoC).	Mr.V.Shankar
	20251A0462		
	20251A0479		
	20251A04C0		

BTECH 2022-23 (19-23 BATCH)

	Roll No.	Title of the Project	Name of the Supervisor
A3	19251A0450	Implementation of Digital alarm clock with Artix-7 FPGA	Dr. K. Ragini
	19251A0405		
	19251A0424		
	19251A0418		
B7	20251A0463	Design of C-DAC for 16-bit 2 MSPS SAR ADC using Verilog	Dr. K. Ragini
	20251A04A8		
	21255A0410		
	20251A04B8		
B6	20251A0492	Traffic Sign Classification using Tensorflow and Deployment on to ASIC for Engineering Application	G.Krishna Kishore
	20251A0475		
	20251A0482		
	20251A0493		
B18	19251A04A5	Implementation of High Speed Serial I/O using Xilinx tools in FPGA	Mrs.M.Shanthi
	19251A04A6		

BTECH 2017-21 (20-21 BTECH)

Batch No.	Roll No.	Title of the Project	Name of the Supervisor
B8	17251A0485	Delay Estimation of VLSI Circuits Through RC Time Constant using Machine Learning	Mrs.A.Deepthi
	17251A04B9		
	17251A04B0		
	17251A0486		

MTECH (2021-23 BATCH)

Batch No.	Roll No.	Title of the Project	Name of the Supervisor
1.	21251DB101	Design of high performance core micro architecture based on RISC-VISA	Dr. K. Ragini
2.	21251DB102	VLSI design of an Area Efficient Nano AES	Dr. K. Ragini

MTECH (20-22 BATCH)

Batch No.	Roll No.	Title of the Project	Name of the Supervisor
1.	20251DB103	Design and implementation of Reordered Normal basis finite field multiplier using NP Domino logic	Dr. K. Ragini
2.	20251DB104	Implementation of High speed Unbiased rounding for 64 bit Inexact speculative Hub Floating-point Adder and Subtractor	Dr. K. Ragini
3.	20251DB105	Design and Implementation of 32 bit Area efficient,Low power booth Wallace Multiplier on FPGA	V.Radha Krishna
4.	20251DB106	Constant-time synchronous binary counter with minimal clock period	V. Shankar
5.	20251DB111	Error Detection and Correction of SRAM based Terinary content Addressable Memory	B.Sreekanth Reddy
6.	20251DB103	Reversible Random Access Memory With Improved Quantum	Dr. K.Ragini
7.	20251DB104	Design of inexact speculative adder for high speed	Dr. K.Ragini
8.	20251DB105	Design of low power 16-bit carry select adder using binary to excess-1 converter	V.Radha Krishna
9.	20251DB106	Self repairing full adder circuit	A.Deepthi

MTECH (19-21 BATCH)

Batch No.	Roll No.	Title of the Project	Name of the Supervisor
1.	19251DB102	Design of Modified Dual- Coupled Linear Congruential Generator Method Architecture for Pseudo random bit Genaration	V.Shankar
2.	19251DB105	Design of Reversible unsigned multiplier using Wallace tree method	Dr.K.Ragini
3.	19251DB106	Key Based Dynamic Obfuscation of digital circuits for Hardware security	A.Deepthi
4.	19251DB108	Design of Low power Linear Feedback Shift Register	B.Sreekanth Reddy
5.	19251DB113	Design of High Performance Approximate redundant binary multiplier using 4:2,5:2& 7:2 compressors	Dr.K.Ragini
6.	19251DB115	Design of Digital Comparator with multiple inputs	V.Radhakrishna

MTECH (18-20 BATCH) MAJOR PROJECTS

Batch No.	Roll No.	Title of the Project	Name of the Supervisor
1.	18251D3806	Design and Implementation of Ternary Gates for VLSI Circuits	Dr.K.Ragini
2.	18251D3807	Design and Implementation of Approximate Adders to Optimize Power and Area	A.Deepthi

MTECH (17-19 BATCH) MAJOR PROJECTS

Batch No.	Roll No.	Title of the Project	Name of the Supervisor
1.	17251D3805	Design and Implementation of 4x4 Bit Multiplier using Dadda Algorithm and Hybrid Full Adder	Dr. K. Ragini
2.	17251D3806	Design And Implementation Of Multibit Flop-Flop With Data Driven Clock Gating	V Shankar
3.	17251D3809	Low-Power and High Speed Full Adder By Using New XOR And XNOR Gates	Dr. K. Ragini
4.	17251D3813	Implementation Of Secure Cryptographic Key Technique For DES Algorithm using Verilog HDL	B Sreekanth Reddy

Best academic projects from the VLSI Design lab fortheacademicyear2020-21

S.No.	Project Title	Roll Nos	Description
1	Design of high performance core micro architecture based on RISC-VISA	21251DB101	2nd Prize
2	Design and implementation of Reordered Normal basis finite field multiplier using NP Domino logic	20251DB103	1st Prize
3	Speculative Adder for High-Design of Inexact Speed and Low Power Applications	20251DBI044	1st Prize
4	Implement of 4-bit ALU with | Logical Obfuscation	19251DB106	2nd prize
5	Low-Power and High Speed Full Adder by using New XOR and XNOR gates	17251D3809	1st Prize

Outcome of the Student Academic projects

Papers published/communicated

S.No	Title of the Paper	Name of the Conference/Journal	Conference Dates	Status of the paper(Submiited/Accepted/Published)
1.	Implementation of 64-bit Inexact Speculative half unit based Floating point Adder	Dr.K.Ragini	2023	Published
2. .	Analysis of Serial-in Parallel-out finite field multiplier using various Domino Logic Styles	Dr.K.Ragini	2023	Published
3.	DNA based AES algorithm using Verilog HDL	P. Roopa Ranjani	2023	Published
4.	Implementation of High-Speed Serial I/O using Xilinx Tools in FPGA	M. Shanthi	2023	Published

5. .	Design of 32x32 Reversible Unsigned Multiplier Using Dadda Tree Algorithm	Dr.K.Ragini	2022	Published
6.	VLSI Implementation of High-Performance Ternary Operand PPA for FIR Filter Application	V.Radha Krishna	2022	Published
7.	AES Algorithm for secure Electrocardiogram(ECG) Signal Transmission	P. Roopa Ranjani	2022	Published
8. .	Design of 4x4 Reversible Multiplier using Reversible TSG Gate	Dr.K.Ragini	2021	Published
9.	Design of digital Comparator with Multiple inputs	V.Radha Krishna	2021	Published
10.	Design of Linear Feedback Shift Register for Low Power Applications	B.Sreekanth Reddy	2021	Published
11. .	Design and Implementation of Ternary logic circuits for VLSI Applications	Dr.K.Ragini	2020	Published
12.	A review paper on games designed and implemented on FPGA	V.Radha Krishna	2020	Published
13.	Multi-stage Threshold Method for Liver Tumor Segmentation in CT Scan Images and Its Implementation for FPGA	B.Sreekanth Reddy	2020	Published
14. .	Low power and high speed full adder using new XOR and XNOR gates	Dr.K.Ragini	2019	Published
15. .	Design of a New Subthreshold-Level Shifter Using Self-controlled Current Limiter	Dr.K.Ragini	2019	Published
16.	Implementation of secure cryptographic key techniques for DES algorithm using Verilog HDL	B.Sreekanth Reddy	2019	Published
17.	Design and Implementation of sum of absolute difference for variable block size motion estimation in video coding	V.Shankar	2019	Published

18. .	Design and Implementation of 4x4 bit multiplier using DADDA algorithm	Dr.K.Ragini	2018	Published
19. .	Design of a Novel High-Speed- and Energy-Efficient 32-Bit Carry-Skip Adder	Dr.K.Ragini	2018	Published
20.	Design of a Highly Reliable and Reconfigurable Pulsed Latch Circuits	Dr.K.Ragini	2018	Published
21.	Design of a low power and high speed 512 bit shift register using static differential sense amplifier shared pulsed latch circuit	Dr.K.Ragini	2018	Published
22.	Implementation of low power multiplier using approximate 15-4 compressor	B.Sreekanth Reddy	2018	Published
23.	Design of 2-4 decoders and 4-6 decoders using GDI technique	V.Shankar	2018	Published